

Schematic Page Description

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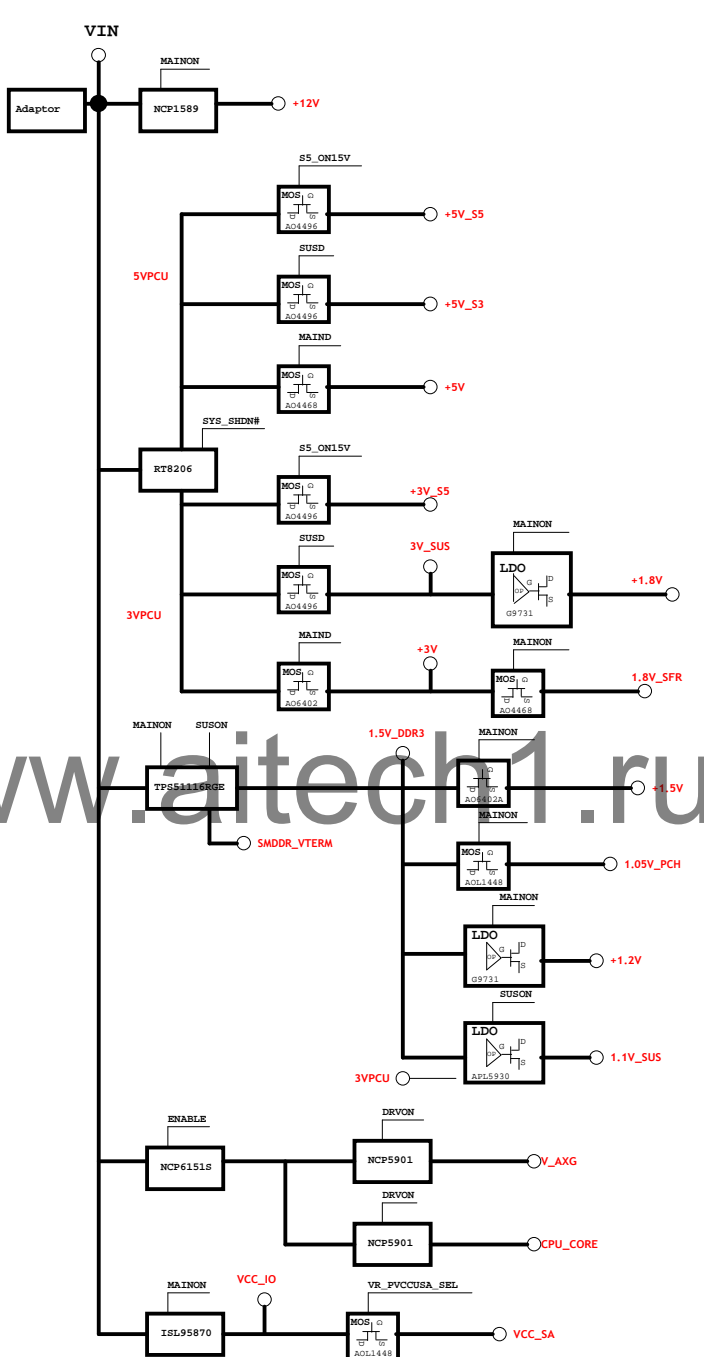
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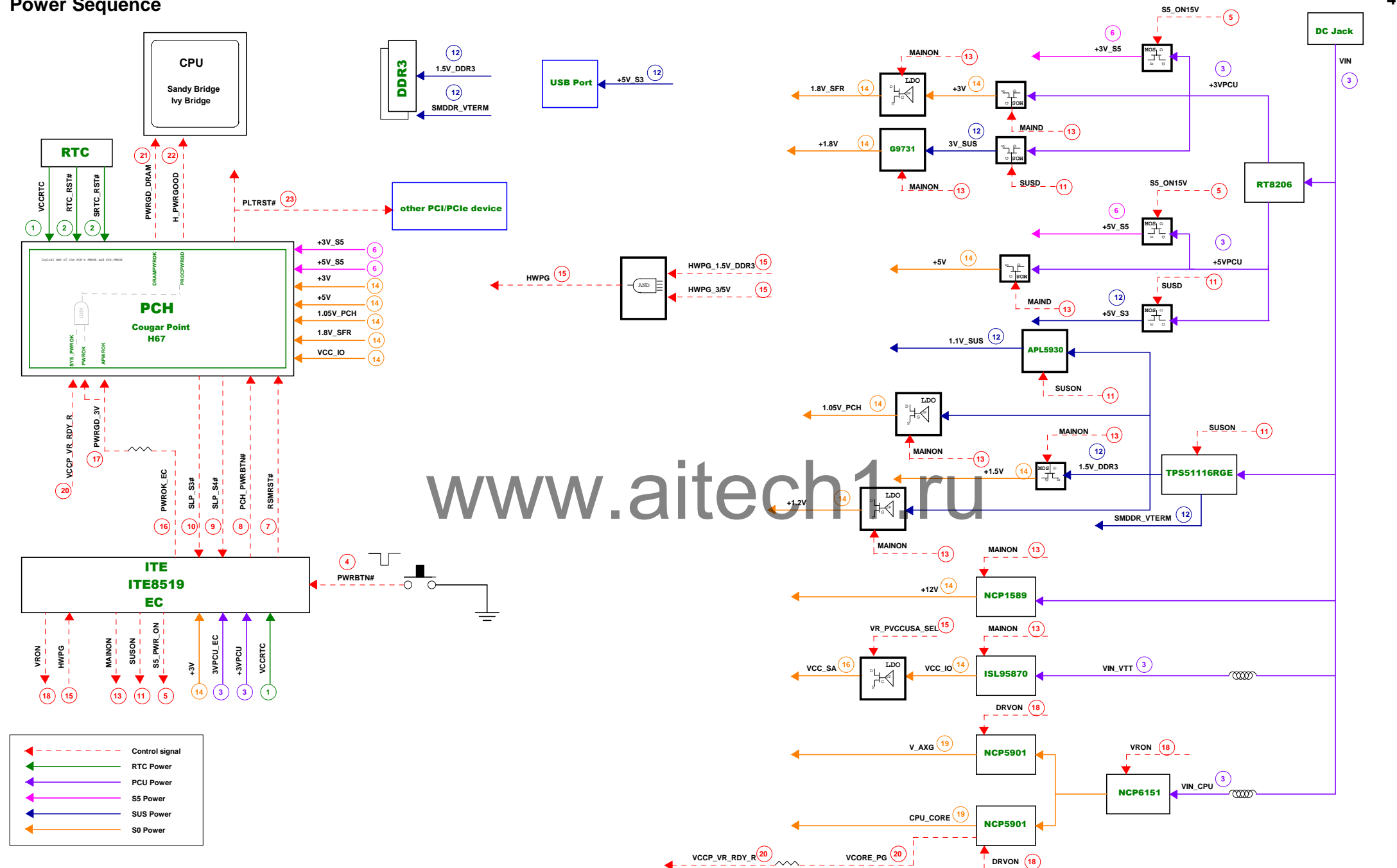
Power Rail	Destination	Voltage		S0 Current
CPU_CORE	Sandy Bridge: CPU core	0.65V-1.3V		112A
V_AXG	Sandy Bridge: CPU AXG	0.5 V-1.3V		35A
VCC_SA	System Agent	0.925 V/0.85 V		8.8A
VCC_IO	Sandy Bridge : Memory controller PCH : DMI PCH : CPU_IO	Hi-->1.05V 1.1V 1.05V-1.1V-1.16V	Low-->1.1V 0.065A 0.001A	8.5A (TDC)
1.8V_SFR	Sandy Bridge: Internal processor PLL PCH : PCH : Dual channel NAND I/F	1.71V-1.8V-1.89V 1.71V-1.8V-1.89V 1.71V-1.8V-1.89V		1.1A 0.196A 0.156A
+1.8V	LAN re-driver			
1.5V_DDR3	Sandy Bridge: CPU I/O Voltage for DDRIII DIMM :	1.425V-1.5V-1.575V		9A 11A
SMDDR_VTERM	DDRIII Terminator:	0.75V		2A
1.05V_PCH	PCH :PCH_1.05V PCH : Vcc core I/O buffer PCH : DMI buffer voltage PCH : Display PLL A power PCH : Display PLL B power	0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V		1.629A 3.251A 0.065A 0.075A 0.075A
+1.5V	Mini PCIE : +1.5V(WLAN)	1.425V-1.5V-1.575V		0.5A
1.1V_SUS				
3V_SUS				
+3V	PCH: I/O buffer voltage PCH: Display DAC Analog power IDT 92HD80 : DVD Mini PCIE : +3.3V(WLAN) CAREMA 3V FOR MXM STDP4010 (M/B) RTS5138	3.14V-3.3V-3.47V 3.135V-3.3V-3.465V 3.102V-3.3V-3.498V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V		0.357A 0.069A 2.75A 1A 0.11A 0.035A
+5V	PCH: Core well Ref. voltage SATA ODD SATA HDD(2.5" x SSD) LCD Panel (SAMSUNG) 5V FOR MXM	4.75V-5V-5.25V 4.75V-5V-5.25V 4.75V-5V-5.25V 4.5V-5V-5.5V 4.7V-5V-5.3V		0.001A 1.5A 0.65A 1.6A 2.5A
+5V_S3	USB: x 12 ports	5V		6A
+12V	SSD HDD FAN_CPU CONVERTER : 12V LCD Panel (LG)	11.4V-12V-12.6V 11.4V-12V-12.6V 12V 11.6V-12V-12.4V		0.46A 0.46A 2A 0.226A 1.08A
+3V_S5	PCH : Intel Management Engine PCH : Suspend well I/O Buffer PCH : HD Audio controller EC(IT8519) : VSTBY SPI FLASH ROM	3.14V-3.3V-3.47V 3.14V-3.3V-3.47V 3.14V-3.3V-3.47V 3.0V-3.3V-3.6V		0.086A 0.168A 0.006A
+5V_S5	PCH : Suspend well Ref. Voltage	4.75V-5V-5.25V		0.001A
3VPCU	EC(IT8519) : VPCU	3.0V-3.3V-3.6V		
5VPCU				
VIN	CONVERTER(SUMSUNG) : Vin CONVERTER : Vin 1.9V FOR MXM	17V-19V-21V 17V-19V-21V 19V		1.1A 1.6A 10A
+1.2V	STDP4010 (M/B)	1.14V-1.2V-1.26V		0.21A



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Power Sequence

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POWER SEQUENCE

Voltage Rails

Power	Voltage	S0	S3	S4	S5	PCU	G3	Ctrl Signal
VCRTC	3V	ON	ON	ON	ON	ON	ON	RTC, PCH
VN	19V	ON	ON	ON	ON	ON	OFF	Adapter In
3VPCU	3V	ON	ON	ON	ON	ON	OFF	Adapter In
3VPCU	3.3V	ON	ON	ON	ON	ON	OFF	Adapter In
+5V_S5	5V	ON	ON	ON	ON	OFF	OFF	SS_PWR_ON
+3V_S5	3.3V	ON	ON	ON	ON	OFF	OFF	SS_PWR_ON
+5V_S3	5V	ON	ON	OFF	OFF	OFF	OFF	SUSD
3V_SUS	3.3V	ON	ON	OFF	OFF	OFF	OFF	SUSD
1.5V_DDR3	1.5V	ON	ON	OFF	OFF	OFF	OFF	SUSON
SMDDR_VTERM	0.75V	ON	ON	OFF	OFF	OFF	OFF	SUSON
1.1V_SUS	1.1V	ON	ON	OFF	OFF	OFF	OFF	SUSON
+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	MAON
+3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	MAON
+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	MAON
+1.5V	1.5V	ON	OFF	OFF	OFF	OFF	OFF	MAON
1.8V_SFR	1.8V	ON	OFF	OFF	OFF	OFF	OFF	MAON
+1.5V	1.5V	ON	OFF	OFF	OFF	OFF	OFF	MAON
1.05V_PCH	1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAON
VCC_IO	1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAON
+1.2V	1.2V	ON	OFF	OFF	OFF	OFF	OFF	MAON
V_A0G	0.5-1.3V	ON	OFF	OFF	OFF	OFF	OFF	VRON
CPU_CORE	0.65-1.3V	ON	OFF	OFF	OFF	OFF	OFF	VRON
VCC_SA	0.925/0.95 V	ON	OFF	OFF	OFF	OFF	OFF	VN_PVCCUSA_SB

Power	Voltage	S0	S3	S4	S5	PCU	G3
3VPCU_EC	3.3V	ON	ON	ON	ON	ON	OFF
VN_CPU	19V	ON	ON	ON	ON	ON	OFF
VN_YIT	19V	ON	ON	ON	ON	ON	OFF
VN_LCD	19V	ON	ON	ON	ON	ON	OFF
USBVCC2	5V	ON	ON	OFF	OFF	OFF	OFF
USB3.0_VCC1	5V	ON	ON	OFF	OFF	OFF	OFF
USB3.0_VCC2	5V	ON	ON	OFF	OFF	OFF	OFF
3V_USB_A	3V	ON	ON	OFF	OFF	OFF	OFF
VN_MXM	19V	ON	OFF	OFF	OFF	OFF	OFF
+5V_MXM	5V	ON	OFF	OFF	OFF	OFF	OFF
+3V_MXM	3.3V	ON	OFF	OFF	OFF	OFF	OFF
+12V_HDD	12V	ON	OFF	OFF	OFF	OFF	OFF
+5V_HDD	5V	ON	OFF	OFF	OFF	OFF	OFF
+12V_SSD	12V	ON	OFF	OFF	OFF	OFF	OFF
+5V_SSD	5V	ON	OFF	OFF	OFF	OFF	OFF
LCDVCC	1.2/5V	ON	OFF	OFF	OFF	OFF	OFF
+5V_Touch	5V	ON	OFF	OFF	OFF	OFF	OFF
CCD_PWR	3.3V	ON	OFF	OFF	OFF	OFF	OFF
VDDA_CODEC	5V	ON	OFF	OFF	OFF	OFF	OFF
+A2A_VDD	3.3V	ON	OFF	OFF	OFF	OFF	OFF
+3V_TV	3.3V	ON	OFF	OFF	OFF	OFF	OFF
VCC3_CARD	3.3V	ON	OFF	OFF	OFF	OFF	OFF

RTC, PCH
 IR Receiver
 EC, Flash
 PCH, AMP, BT
 PCH, G-sensor, XDP, SPI flash ROM
 USB3.0, USB2.0
 DDR3, CPU DDR3 IO
 DDR3
 PCH, CRT, Multi-touch, ODD, HDD, SSD, Buzzer, Panel
 CG7216, CCD, D-Mic, USB controller, WL, TV, RTS5138, Codec, MXM, PCH, DDR3, Flash, EEPROM
 FAN, Panel, HDD, SSD
 LAN re-driver
 PCH, CPU_PLL
 WL, TV
 PCH_IO, PCH, CLK, PCH_PL, PCH_CORE
 XDP, PCH_DMI, PCH_PROG, CPU_IO
 STOP4010
 CPU_A0G
 CPU_Core
 CPU_SA

1.5V_DDR3/SMDDR_VTERM/1.1V_SUS/3V_SUS/+5V_S3

VCC_IO/VCC_SA/+12V/+5V/+3V/1.8V_SFR/+1.8V/+1.5V/1.05V_PCH

EC

Converter/B

USB2.0 port

USB3.0 port

USB3.0 port

USB3.0 controller

MXM

MXM

HDD

HDD

SSD

SSD

Panel_LVDS

Multi_touch

CCD

Codec, Audio jack

Codec

TV card

RTS5138

VCRTC

RTC_RST#

VIN/5VPCU/3VPCU

PWRBTN#

SS_PWR_ON

+3V_S5/+5V_S5

RSMRST#

PCH_SUSCLK

PCH_PWRBTN#

SLP_S4#

SLP_S3#

SUSON

MAON

HWP

PWRON_EC

VRON

CPU_CORE/V_A0G

VCORE_PG

SYS_PWRON/PWRON/APWRON

PCH Clock

PWRGD_DRAM

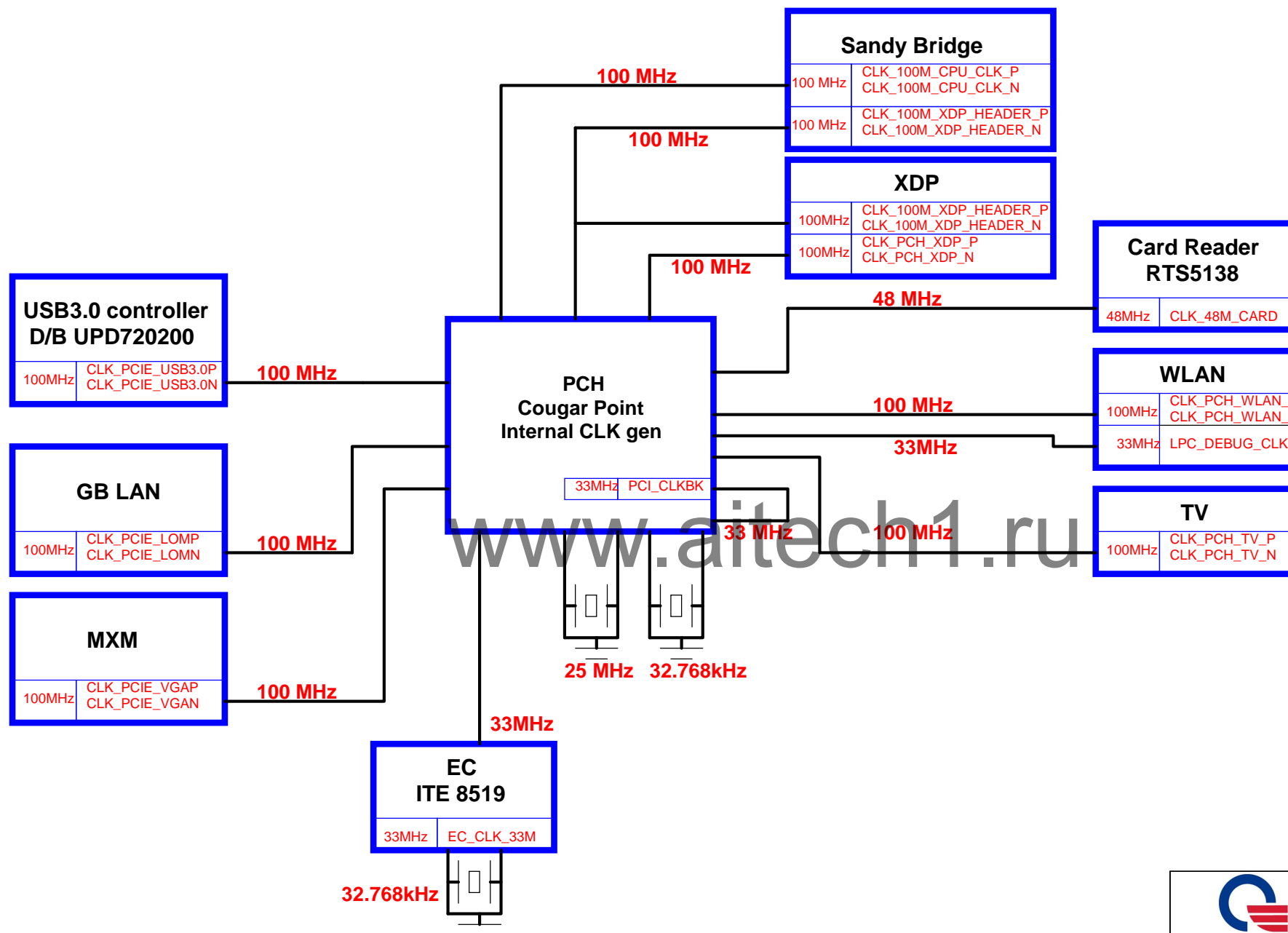
H_PWRGOOD


SUS_STAT#

PLTRST#

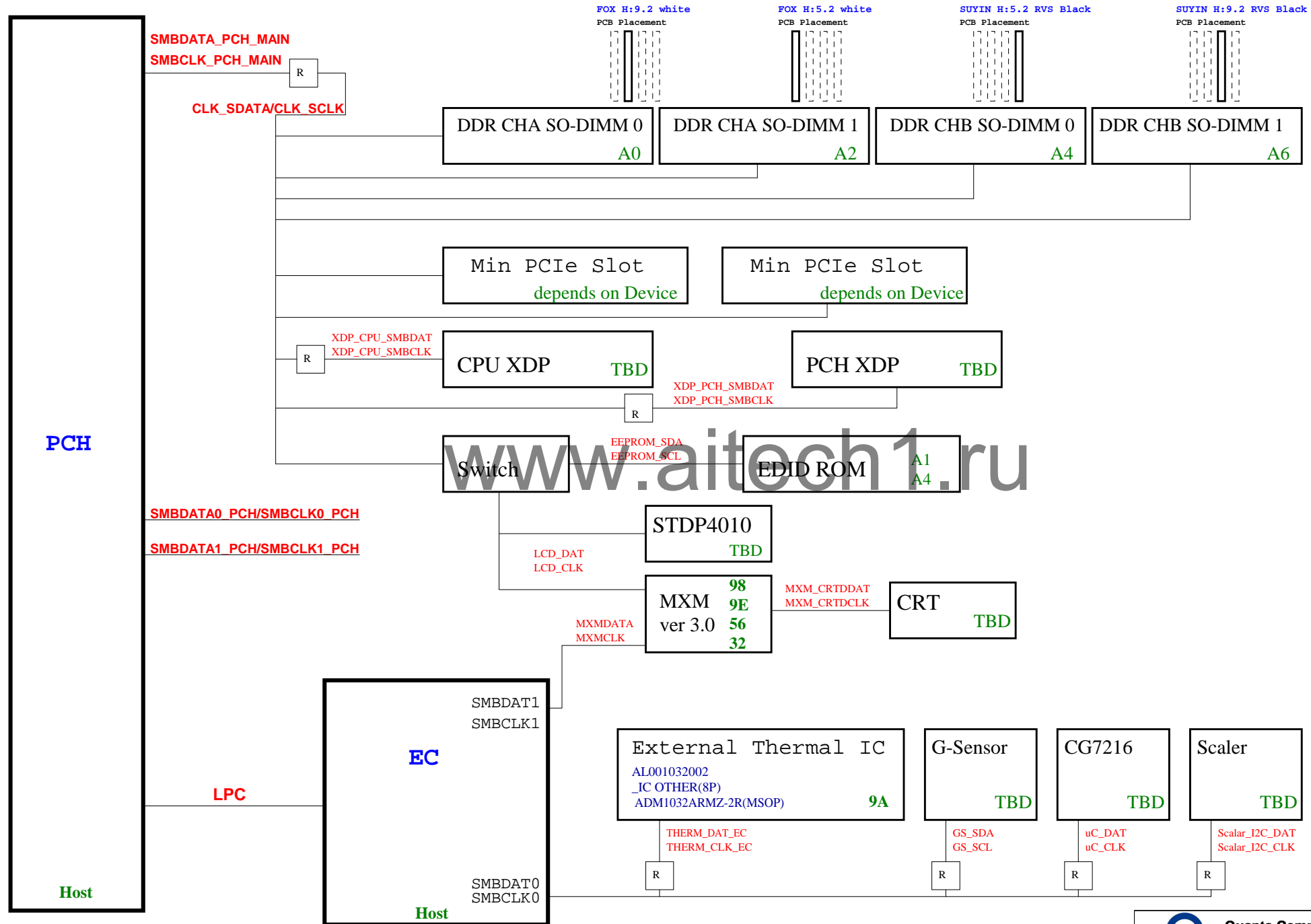
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CLOCK BLOCK DIAGRAM			
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WJ1 SMBus Block Diagram



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NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
		I		INITIAL : HIGH / ACTIVE : LOW
		B		
		I		
		I		
		O		
		O		
		I		
		O		
		O		
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NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
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		I		
		I		
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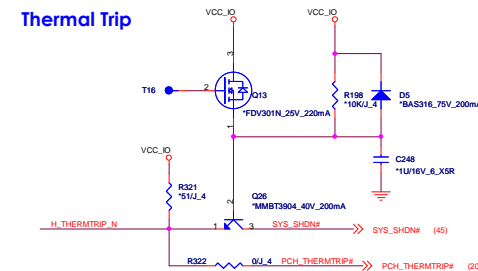
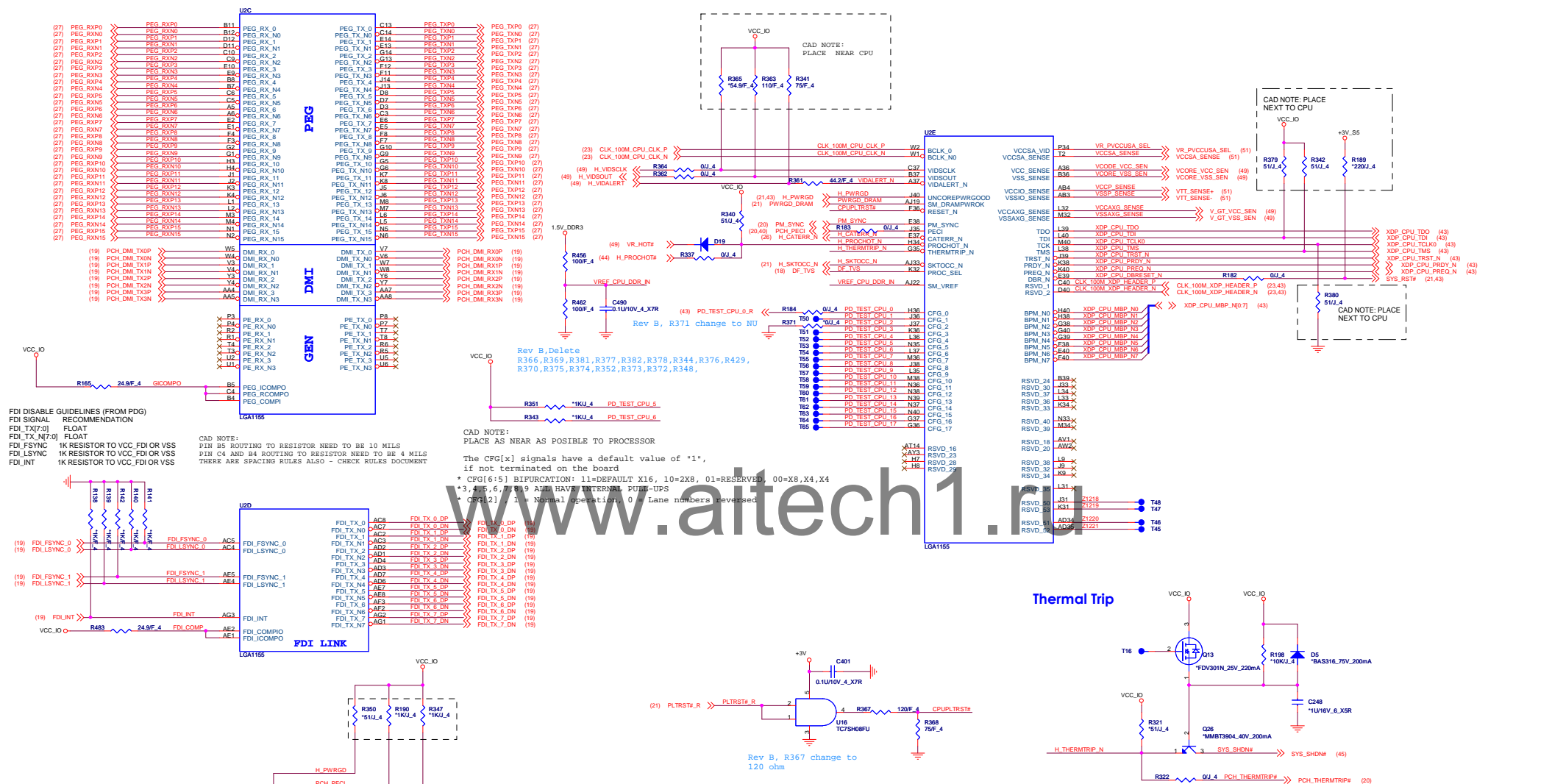


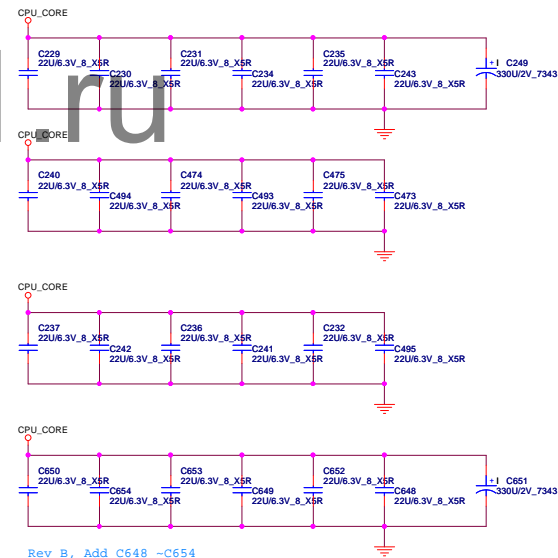
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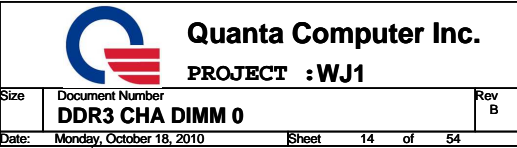
PROJECT : WJ1

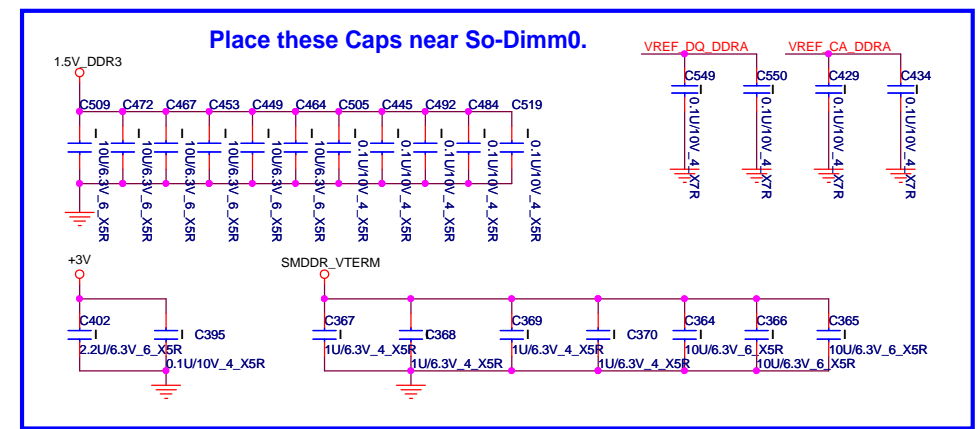
Size	Document Number	Rev
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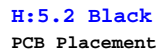
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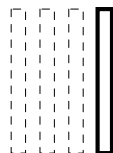


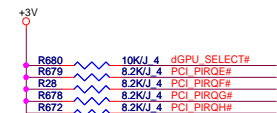
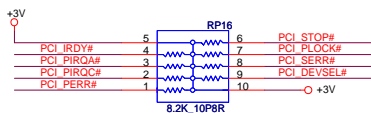
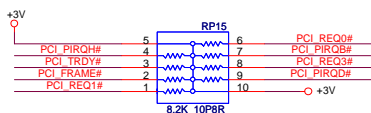
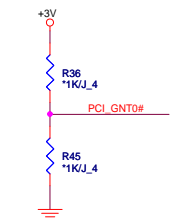
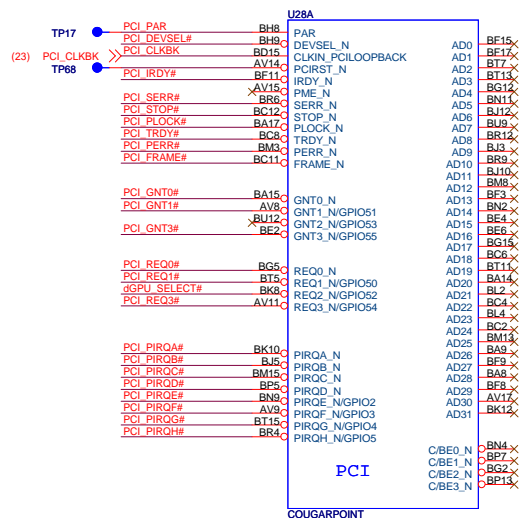


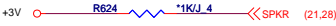



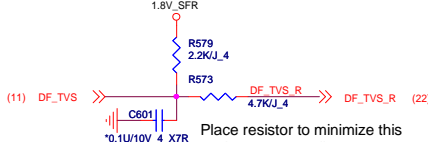






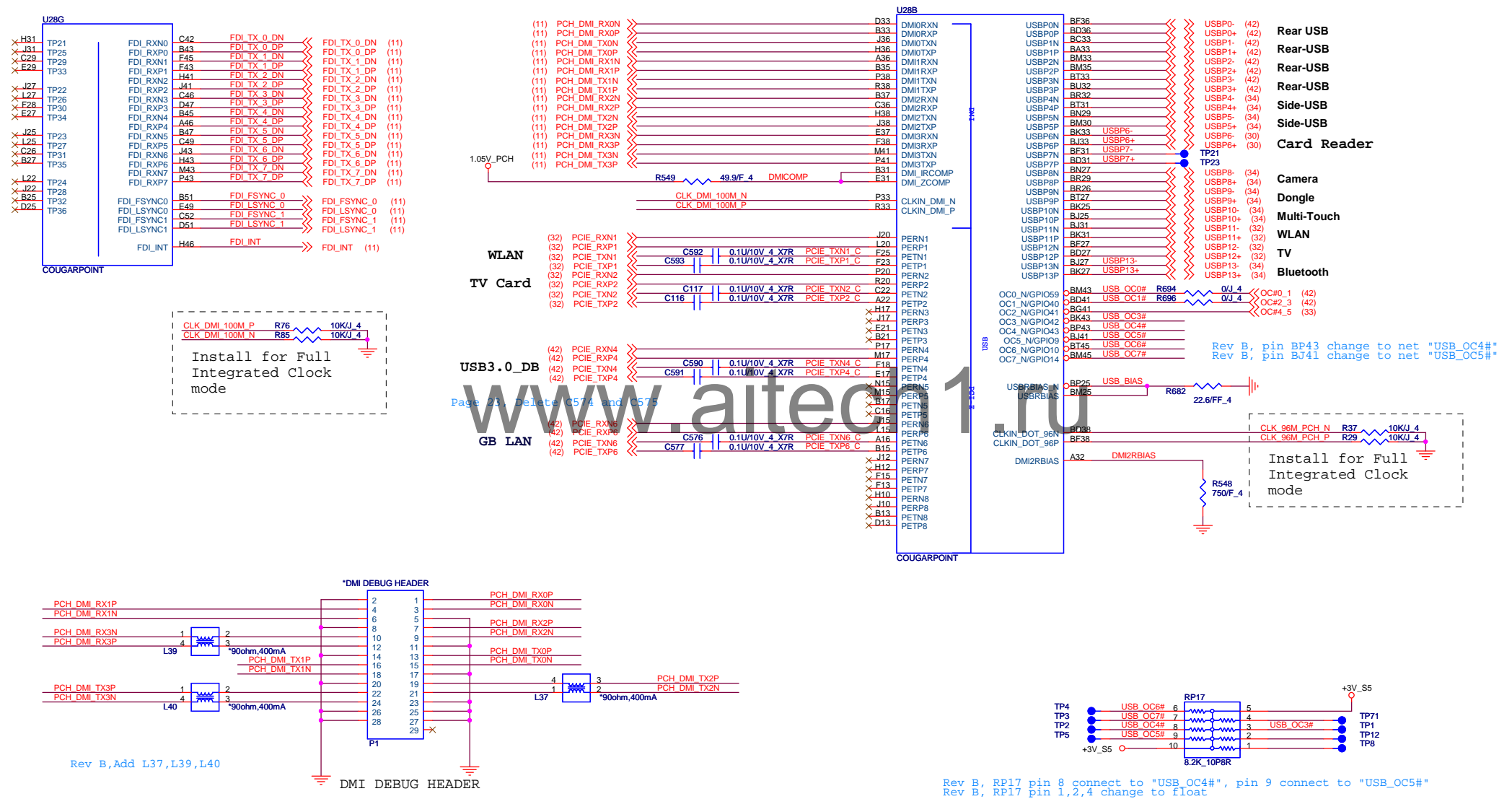


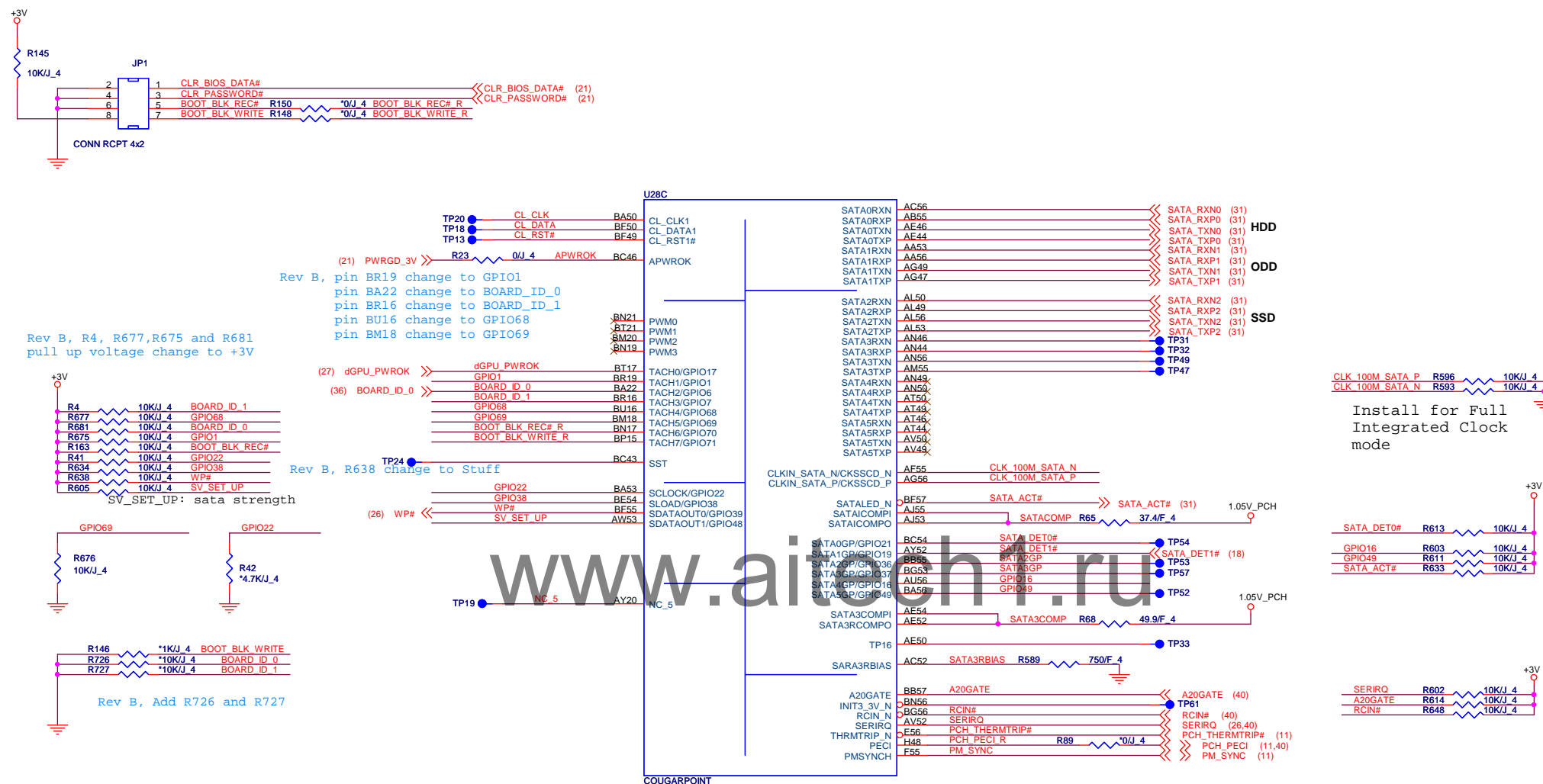
PCH





Pin Name	Strap description	Sampled	Configuration	Note												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V 												
INIT3_3V	Reserved	PWROK	1 = Default (internal weak pull-up) Should not be pull-down	NC												
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	 +3V												
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	VCCRTC  (21)												
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>Bit 1</th><th>Bit 0</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	Bit 1	Bit 0	Boot Location	1	1	SPI	1	0	PCI	0	0	LPC	 (20) WEAK INTERNAL PULLUPS ON GNT#. DEFAULT SPI BOOT DEVICE.
Bit 1	Bit 0	Boot Location														
1	1	SPI														
1	0	PCI														
0	0	LPC														
SATA1GP/GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK														
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Default internal pull up	UNUSE, NC												
HDA_SDO	Flash Descriptor Security Override /ME Debug Mode	REMRST#	0 = Default 1= Override	Use default												
DF_TVS (NV_CLE)	DMI and TDI Termination voltage	PWROK	weak Internal pull-down	 (22) Place resistor to minimize this stub to <= 100 mils												
GPIO28	On die Voltage Regulator	RSMRST#	0 = Disable 1 = Enable(default weak internal pull up)	Use default												
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = Default On die PLL VR supplied by 1.8V 1 = On die PLL VR supplied by 1.5V	use default (0 = 1.8V supply)												
GPIO15	TLS Confidentiality	RSMRST#	0 = Default, Intel ME Crypto TLS with NO confidentiality 1 = Intel ME Crypto TLS with confidentiality	Use default												
SDVO_CTRLDATA	Port B detected	PWROK	0 = Default, not detected 1 = Detected	+3V  (22,36)												
DDPC_CTRLDATA	Port C detected	PWROK	0 = Default, not detected 1 = Detected	+3V  (22)												
DDPD_CTRLDATA	Port D detected	PWROK	0 = Default, not detected 1 = Detected	+3V  (22)												
DSWVRMEN	Deep S4/S5 well on die regulator enable	ALWAYS	0 = Disable 1 = Enable	VCCRTC  (21)												
SATA2GP/GPIO36	Reserved	PWROK	Weak internal pull-down Should not be pull high when sampled	Use default												
SATA3GP/GPIO37	Reserved	PWROK	Weak internal pull-down Should not be pull high when sampled	Use default												
GPIO8	BTM / FCIM		BTM Leave floating FCIM Pull low with 1K to ground	USE BTM												





(28) PCH_AZ_CODEC_RST# << R17 33/J 4 PCH_AZ_CODEC_RST# R
(28) PCH_AZ_CODEC_SDOUT << R9 33/J 4 PCH_AZ_CODEC_SDOUT R
(28) PCH_AZ_CODEC_SYNC << R10 33/J 4 PCH_AZ_CODEC_SYNC R
(28) PCH_AZ_CODEC_BITCLK << R8 22/J 4 PCH_AZ_CODEC_BITCLK R

C20
22P/50V/4

Rev B, R652 pull up voltage change to +3V_S5, NU
Rev B, R19 pull up voltage change to +3V_S5

Rev B, R27, R54 and R659 pull up voltage change to +3V_S5

Rev B, R655, R669, R662, R21 and R53 pull up voltage change to +3V_S5

GPIO28 R652 *10K/J 4
SLP_LAN# R19 *10K/J 4
GPIO67 R666 10K/J 4
R1# R16 10K/J 4
PCIE_WAKE# R33 1K/J 4
BATLOW_N R58 10K/J 4
GPIO27 R5 10K/J 4
GPIO30 R687 10K/J 4
CLR_BIOS_DATA# R27 10K/J 4
CLR_PASSWORD# R54 10K/J 4
GPIO46 R659 10K/J 4
H_SKT0CC_N R662 10K/J 4
EC_SMI# R21 10K/J 4
EC_SCI# R53 10K/J 4
GPIO6 R669 *10K/J 4
USB3.0_SMI_R R655 10K/J 4

Rev B, GPIO12 change to EC_SMI#
Rev B, GPIO13 change to EC_SCI#
Rev B, GPIO44 change to CLR_BIOS_DATA#
Rev B, GPIO45 change to CLR_PASSWORD#

U28D
LDRQ1_N/GPIO23 BA20
FWH0/LAD0 BK15
FWH1/LAD1 BJ17
FWH2/LAD2 BJ20
FWH3/LAD3 BG20
LDRQ0_N BK17
FWH4/LFRAME_N BG10
PCH_DRQ#1 TP15
(26,32,40) LPC_LAD0 << BA20
(26,32,40) LPC_LAD1 << BJ17
(26,32,40) LPC_LAD2 << BJ20
(26,32,40) LPC_LAD3 << BG20
(26,32,40) LPC_LFRAME# << BG10
PCH_DRQ#0 TP67
PCH_AZ_CODEC_BITCLK R BU22
PCH_AZ_CODEC_RST# R BD22
(28) PCH_AZ_CODEC_SDIN0 << BE22
PCH_AZ_CODEC_SYNC R BT23
PCH_AZ_CODEC_SYNC R BT23
PCH_AZ_CODEC_SYNC R BT23

Rev B, Add
R710, R711, R712 and R713

Rev B, R600 change to NU

+3V_S5

VCCRTC R11 1M/F 4

(26) RTC_RST# << TP6
(26) SRTC_RST# << TP6
(40,43) PCH_RSMRST# << TP6
(18) PCH_INTVRMEN << TP6
(18) PCH_DSWMRMEN << TP6

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

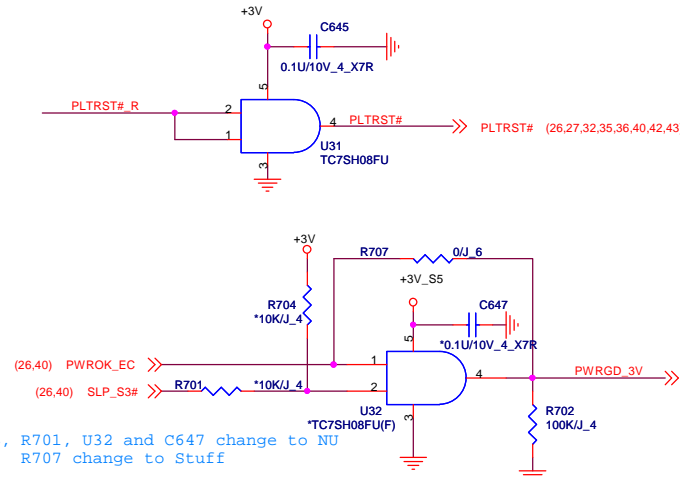
(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69

(26) SMBCLK_PCH_MAIN << TP69
(26) SMBDATA_PCH_MAIN << TP69
(41) SML1ALERT# << TP69



Rev B, C642 and C643 change to 12p

Rev B, R701, U32 and C647 change to NU
R707 change to Stuff

AW55 BMBUSY# TP51
BC56 GPIO32 TP11
BC25 HDA_DOCK_EN# TP59
BL56 GPIO34
BJ57 WRITE_EDID_ROM (37)
GPIO8 BP51
BK50 EC_SMI# TP66
BA25 EC_SCI# (26,40)
BM55 USB3.0_SMI_R (42)
BP53 H_SKT0CC_N (11)
BJ55 GPIO28
BH49 SLP_LAN# TP9
AV43 GPIO20
BL54 CLR_BIOS_DATA# (20)
AV44 CLR_PASSWORD# (20)
BP55 GPIO46
BT53 GPIO57
BJ53 VCCP_VR_RDY_R TP64
BJ48 R1#
BK48 PLTRST# R (11)
BC44 SLP_A# (32,42)
BC41 SLP_S3# (26,40)
BM52 SLP_S4# (26,40)
BH50 SLP_S5# TP14
BN54 SUS_STAT# TP63
BA47 SUSCLK/GPIO62 TP27
AV46 BATLOW_N
BP45 SUSACK_N
BU46 GPIO30
BG46
GPIO27 BJ43
R22 dGPU_PSRNT# (27,35,40)
BD43 SLP_SUS TP16
BT43 PCH_PWRBTN# (40,43)
BE52 SYS_RST# (11,43)
BE56 SPKR (18,28)
D53 H_PWRGD_R R560 0/J 4 >> H_PWRGD (11,43)
TP22 TP_PCH_PMTEST_RST
BA43 XDP_PCH_TCK0 (43)
BC52 XDP_PCH_TDI (43)
BF47 XDP_PCH_TDO (43)
BC50 XDP_PCH_TMS (43)

Rev B, Delete R629

Rev B, R604 change to Stuff
Rev B, Add R737, NU

dGPU_PSRNT# R18 10K/J 4

SW1
SYS_RST# 1 2 3 4 5

RST# BTN

Rev B, SW1 change footprint

PCH_RSMRST# R13 10K/J 4
VCCP_VR_RDY_R R647 *10K/J 4

Rev B, U30 change footprint

R671 4.7K/J 4
C67 0.1U/10V_4_X5R

U30
XDP_VR_READY (43) >> VCCP_PWRGD_R >> VCCP_VR_RDY_R

R670 0/J 4
C638 0.22U/6.3V_4_X5R

Rev B, U30 change footprint

Rev B, U30 change footprint

Rev B, U30 change footprint

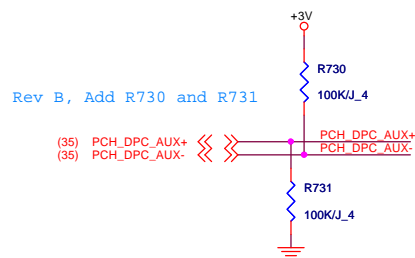
Rev B, U30 change footprint

Rev B, U30 change footprint

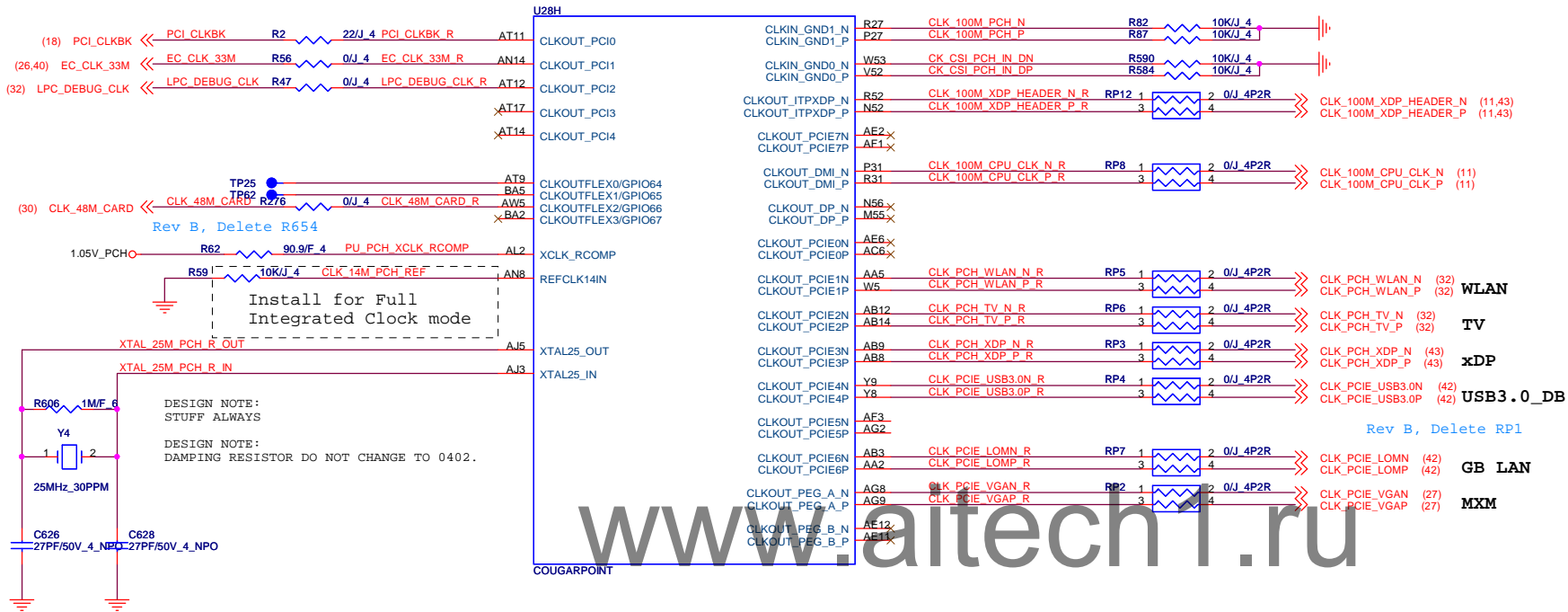
Rev B, U30 change footprint

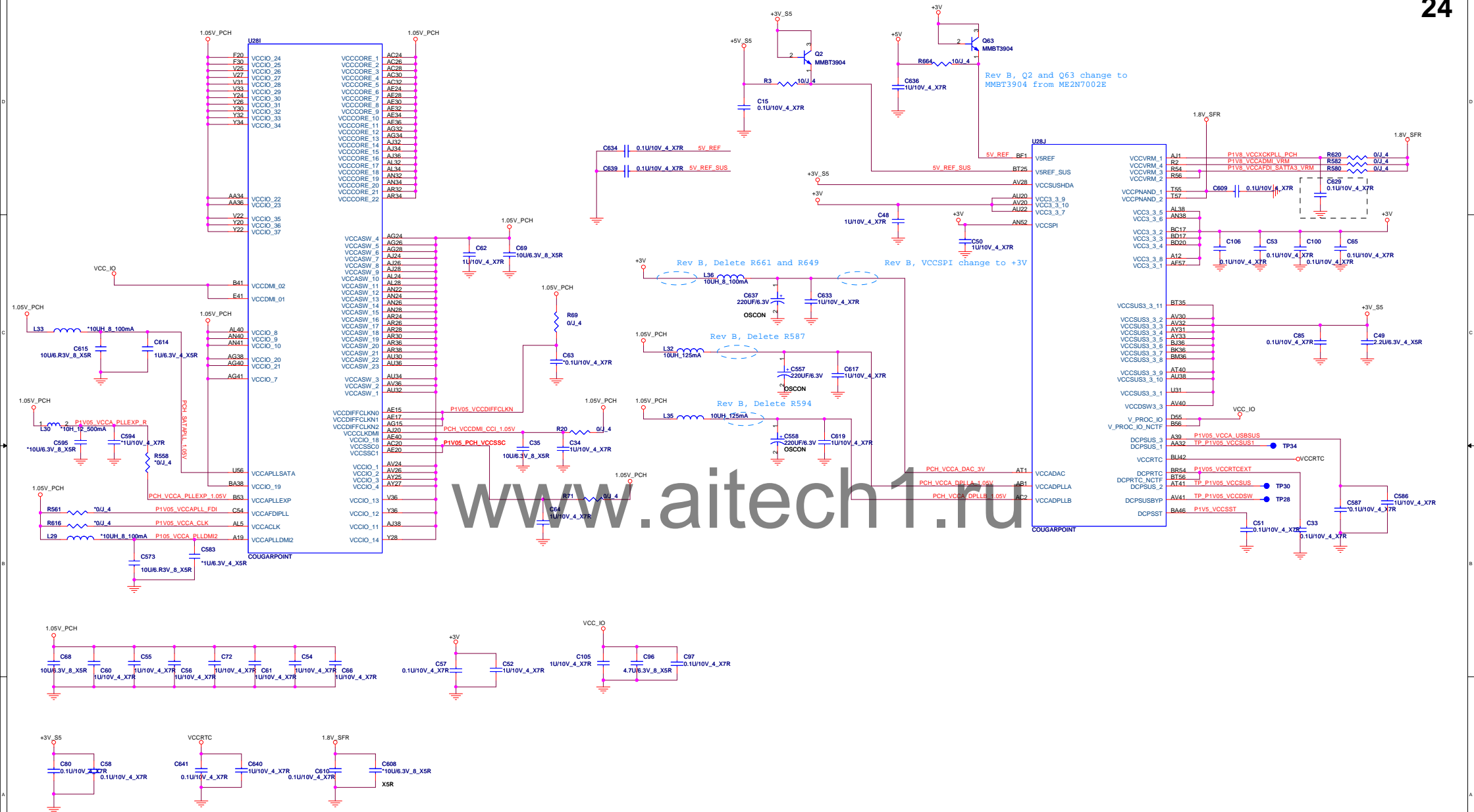
Rev B, U30 change footprint

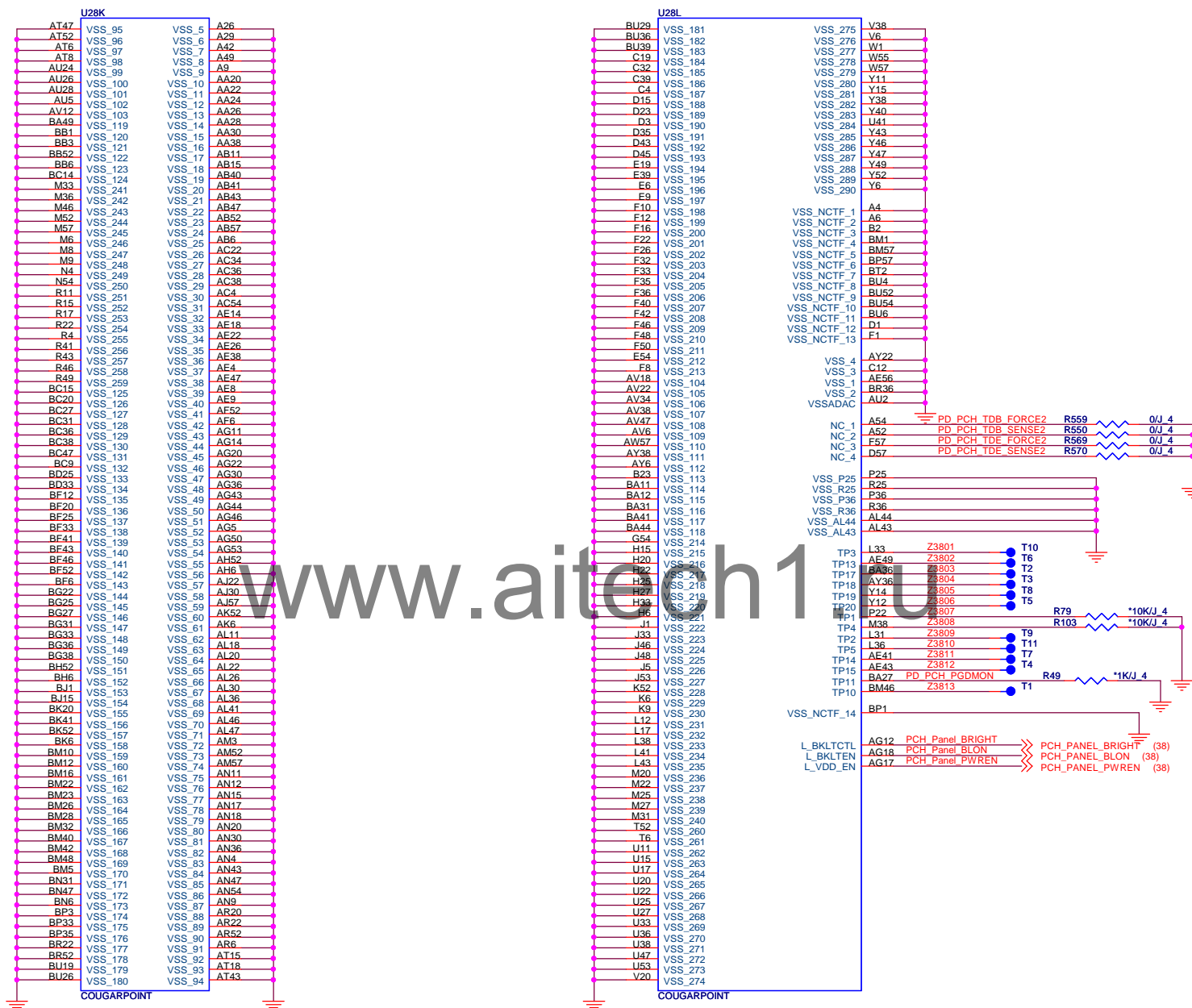
Rev B, U30 change footprint

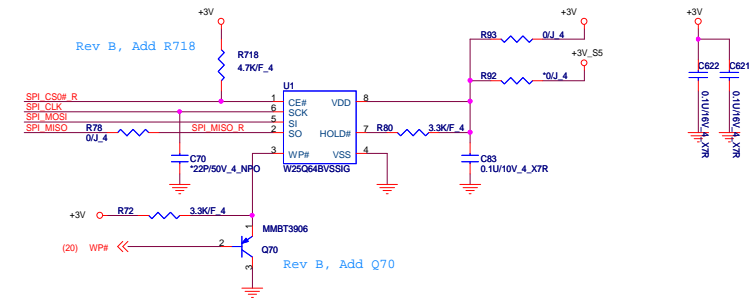
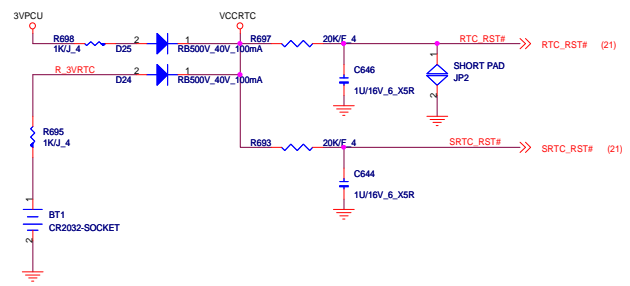


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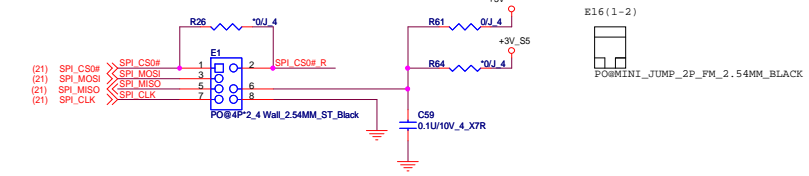




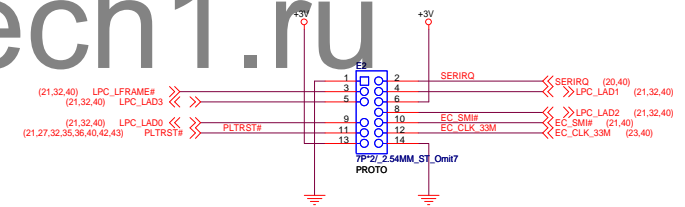




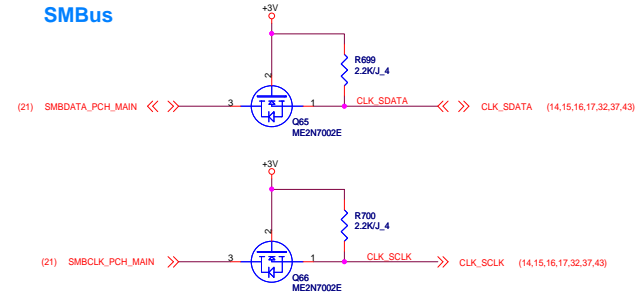
ROM recovery



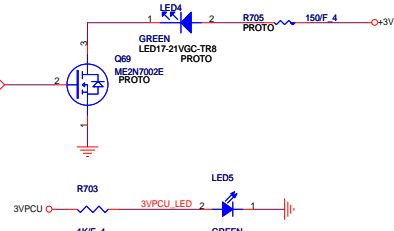
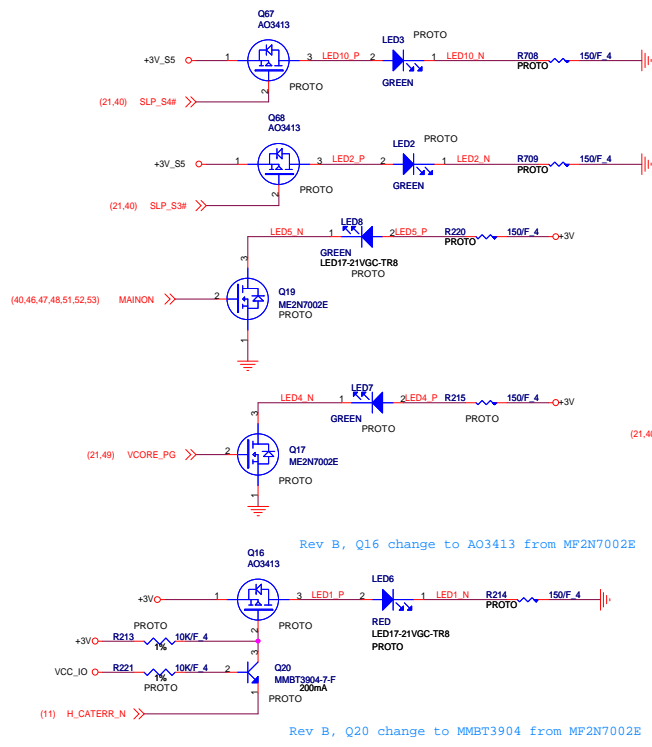
LPC HEADER



SMBus

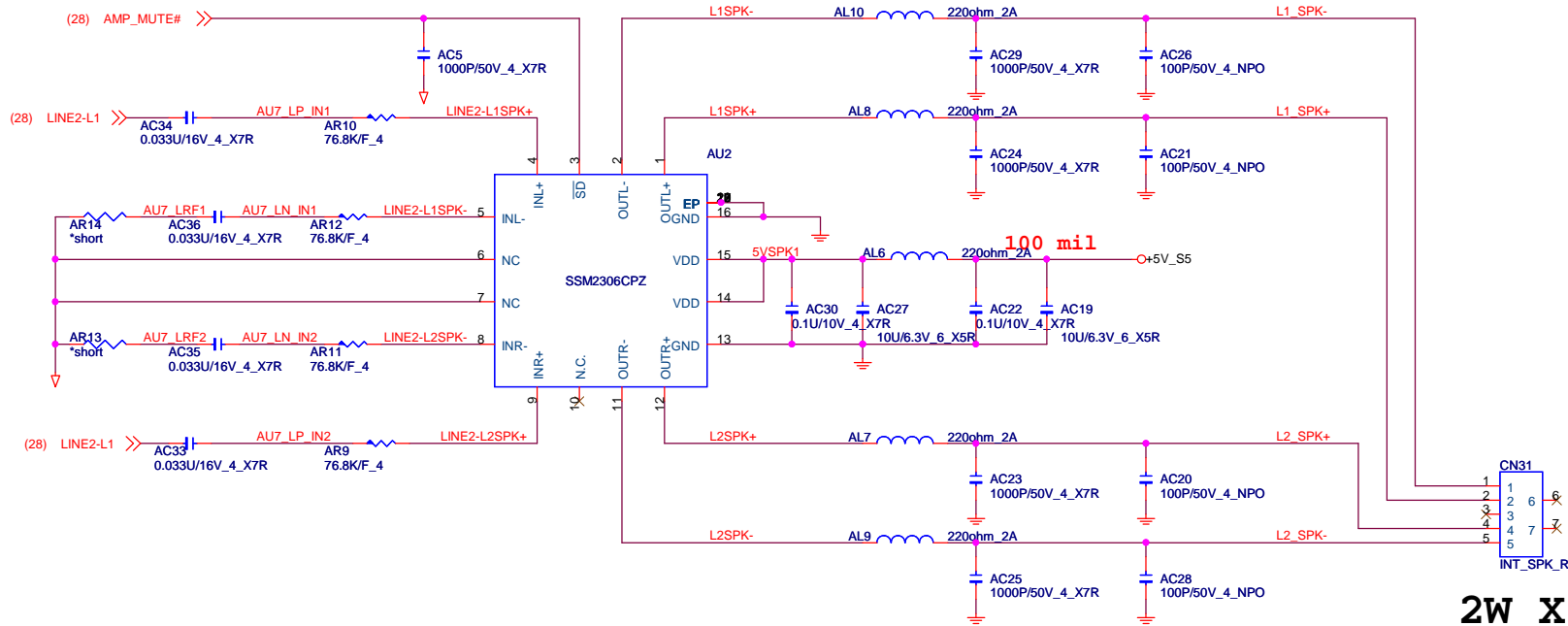


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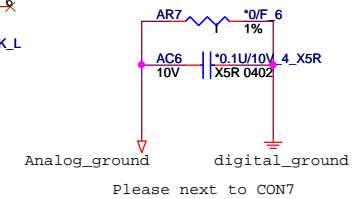
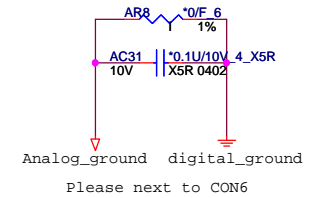




AUDIO AMPLIFIER



2W X 4



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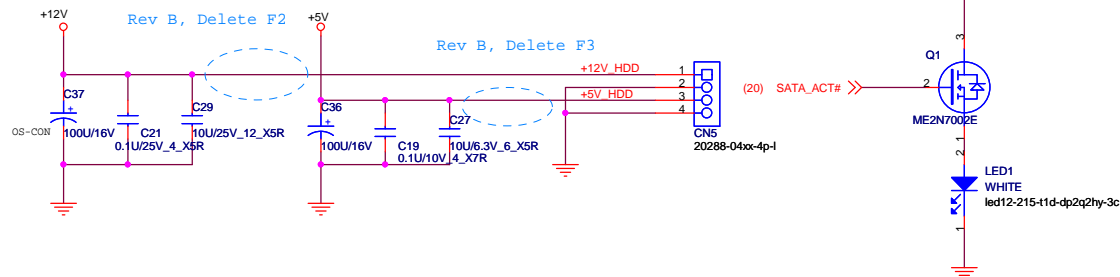
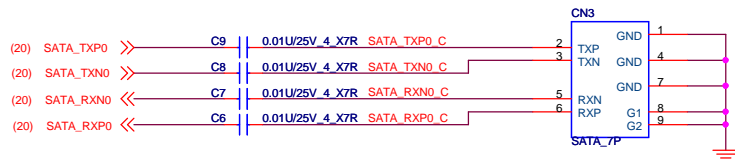
PROJECT : WJ1

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	AMP (SSM2306)	A
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SATA HDD CONNECTOR

From PCH SATA

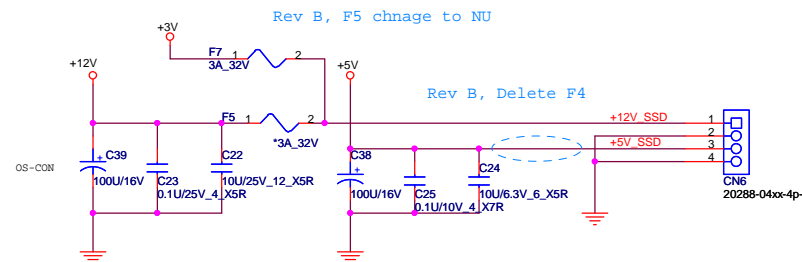
CAP. Close connect side



SATA SSD CONNECTOR

From PCH SATA

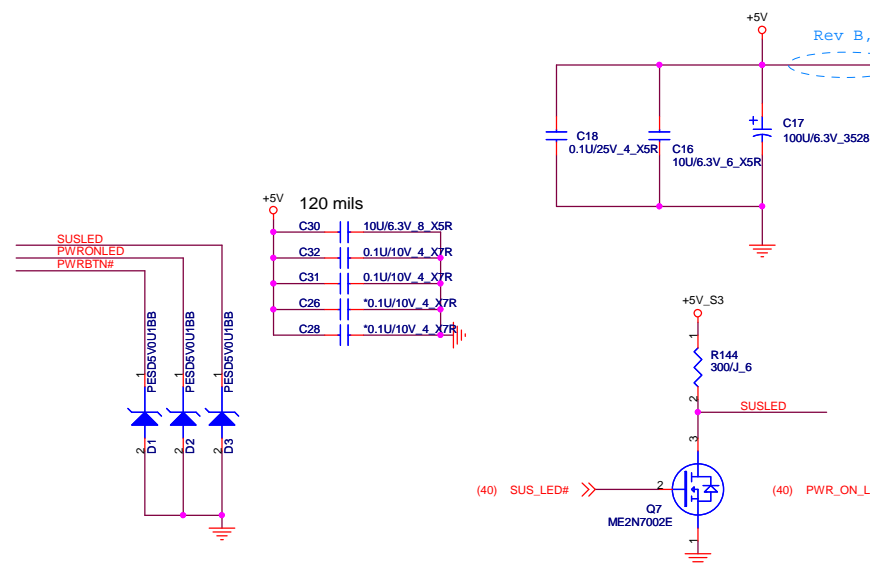
CAP. Close connect side



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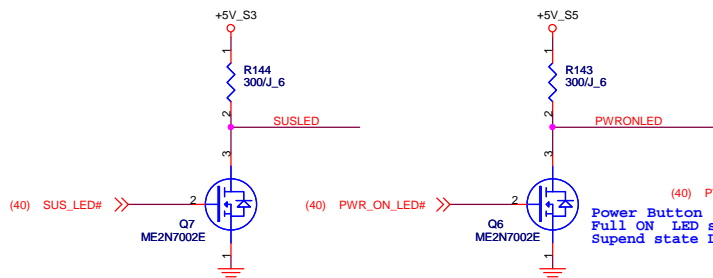
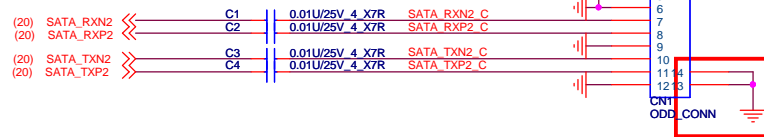
SATA CD-ROM

Rev B, Delete F1



SATA ODD CONNECTOR

USB connector same as ZN6

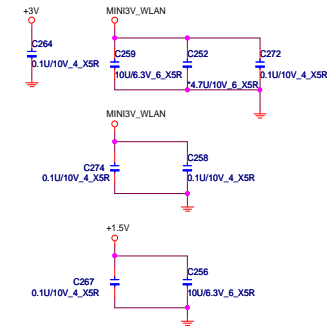
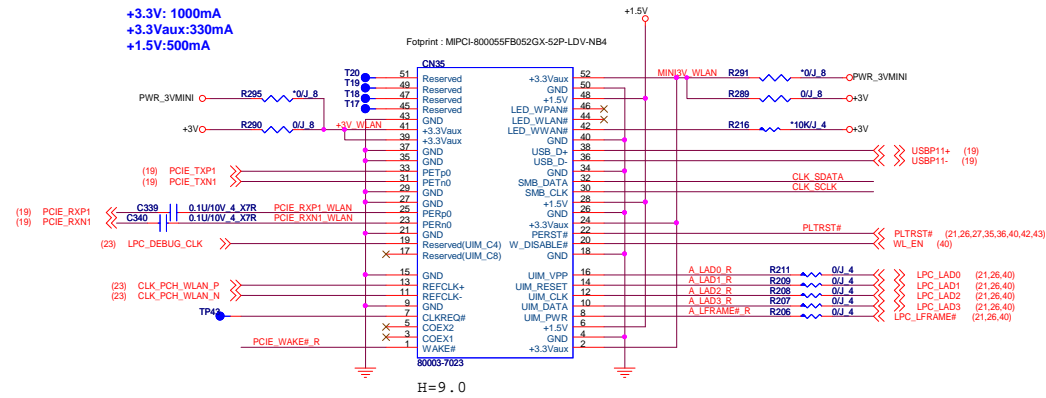


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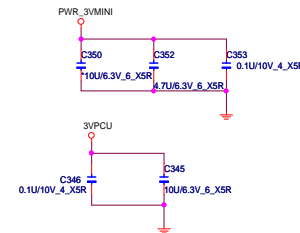
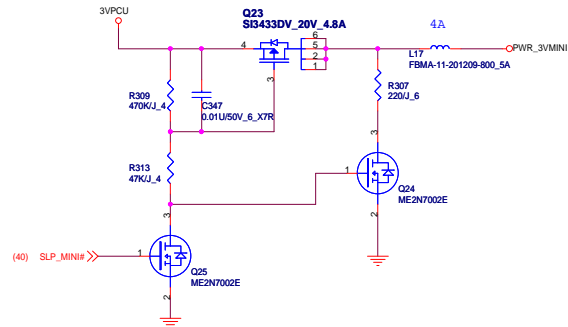
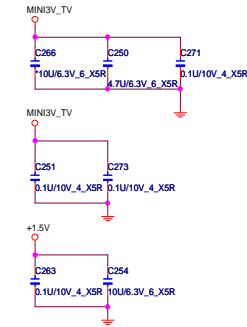
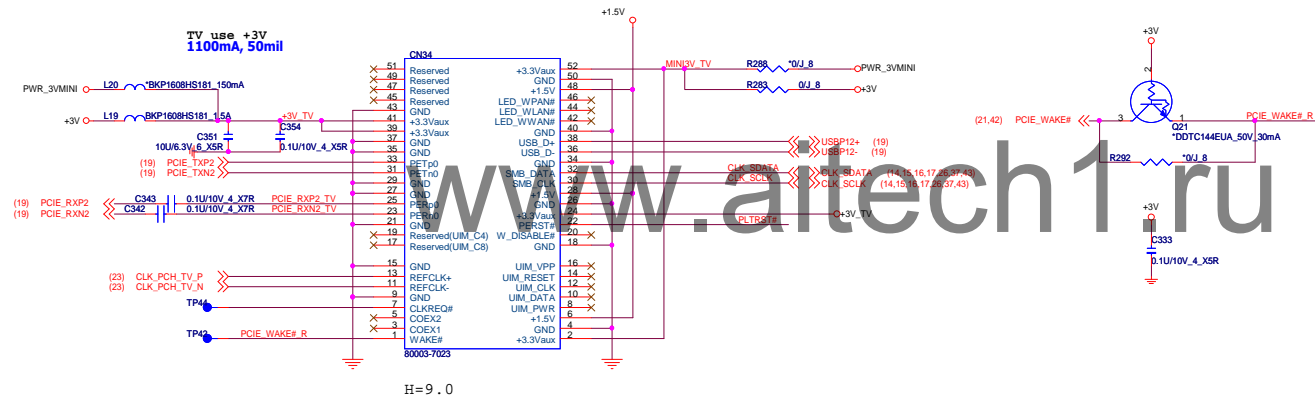
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PROJECT : WJ1

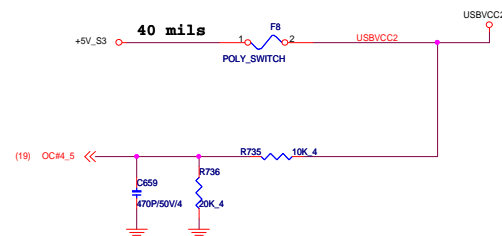
Size Document Number
SATA HDD/ODD/SSD

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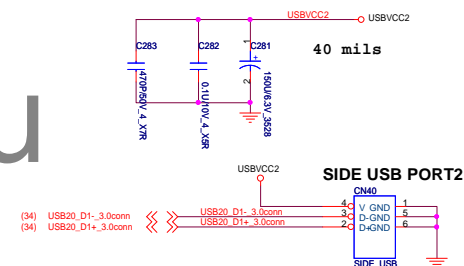
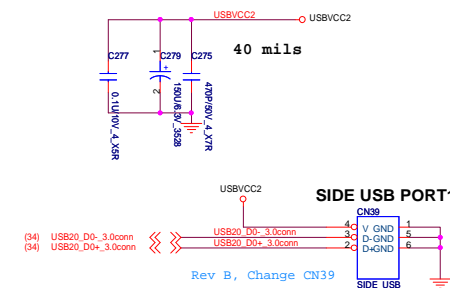


TV

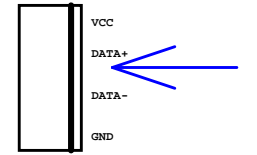
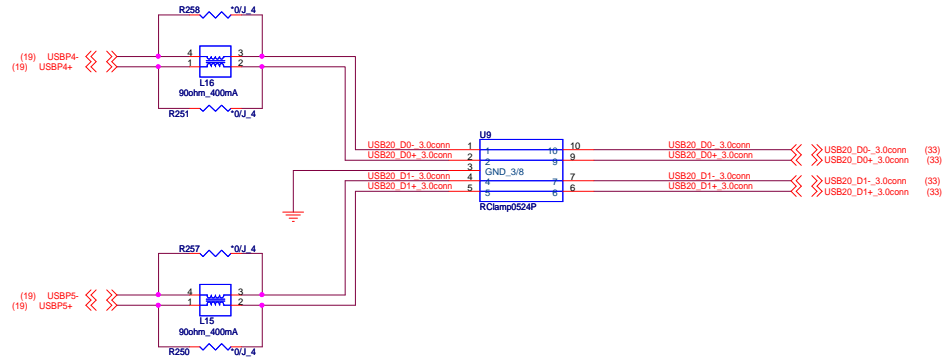




Rev B, Add F8,R735,R736 and C659



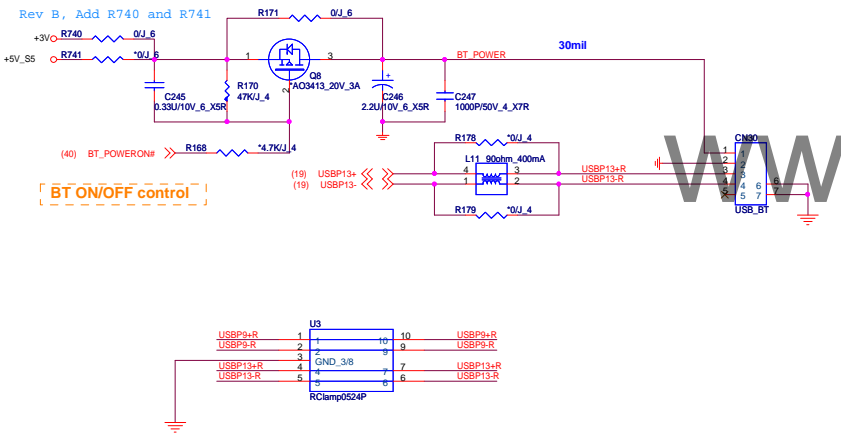
Rev B, Delete C331, R273, R275 and R228



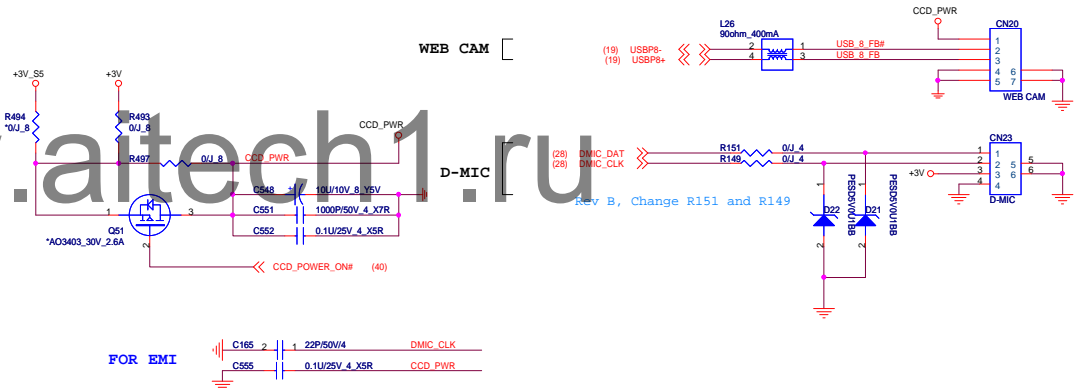
USB connector same as ZN6

BLUETOOTH CONNECTOR

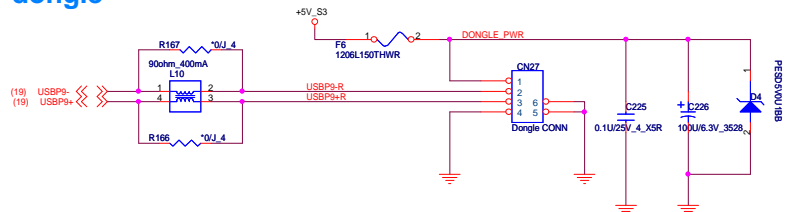
Rev B, Add R740 and R741



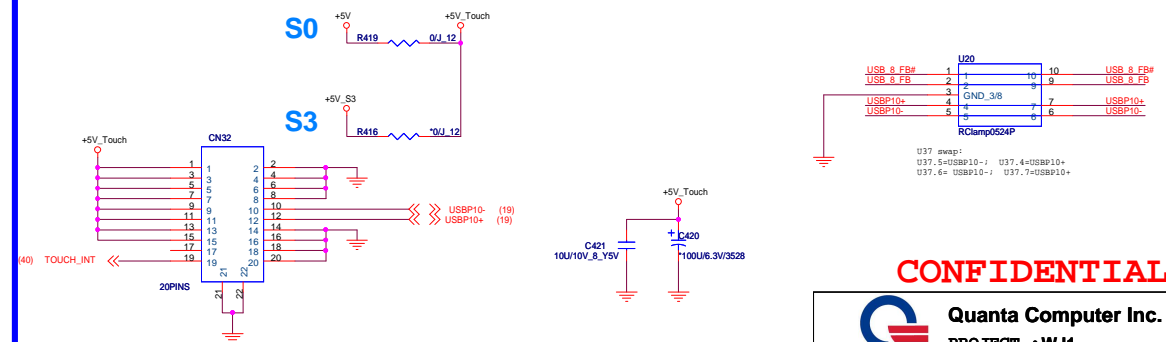
WEB CAM MODULE



For dongle



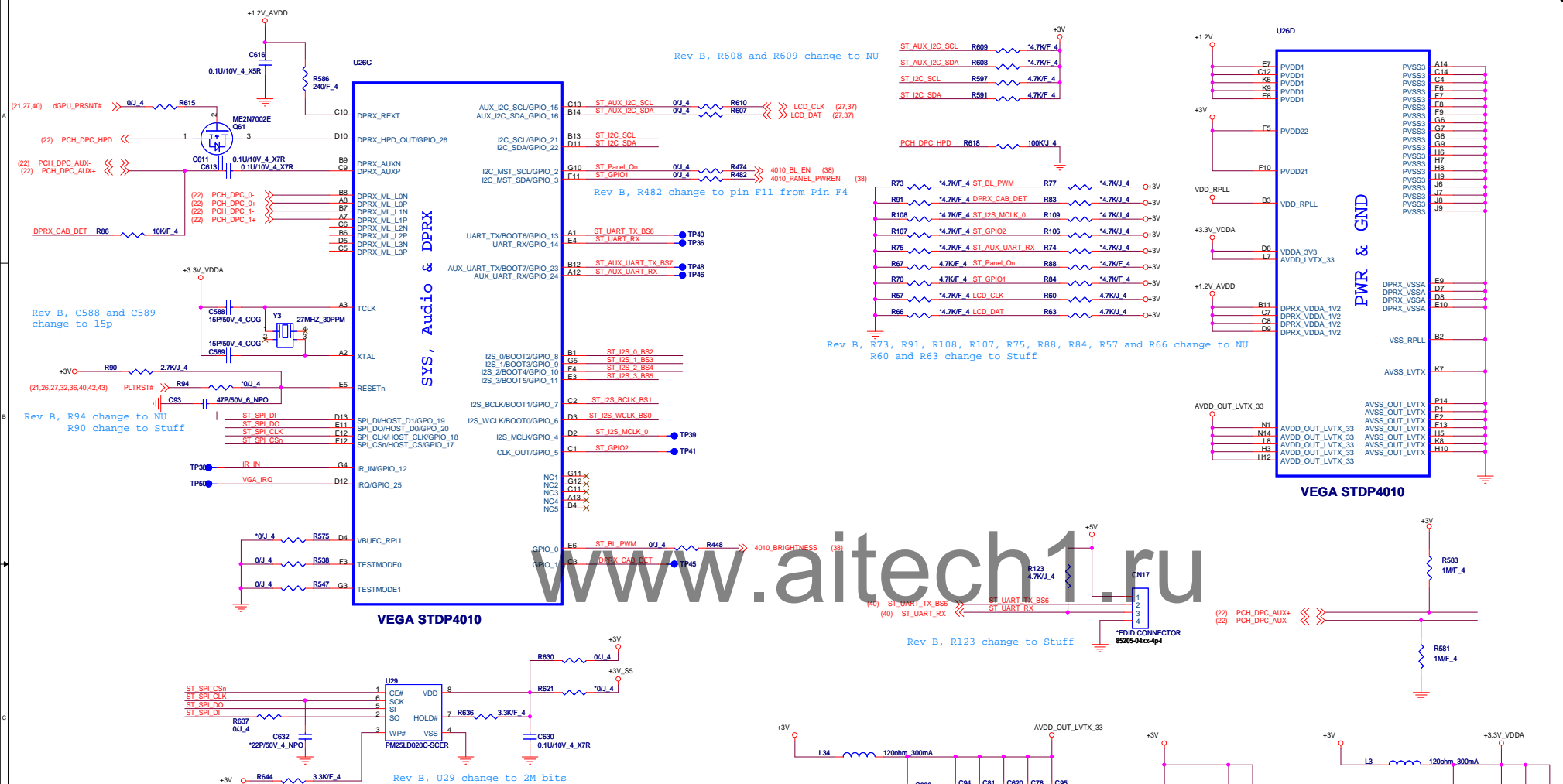
MULTI-TOUCH



















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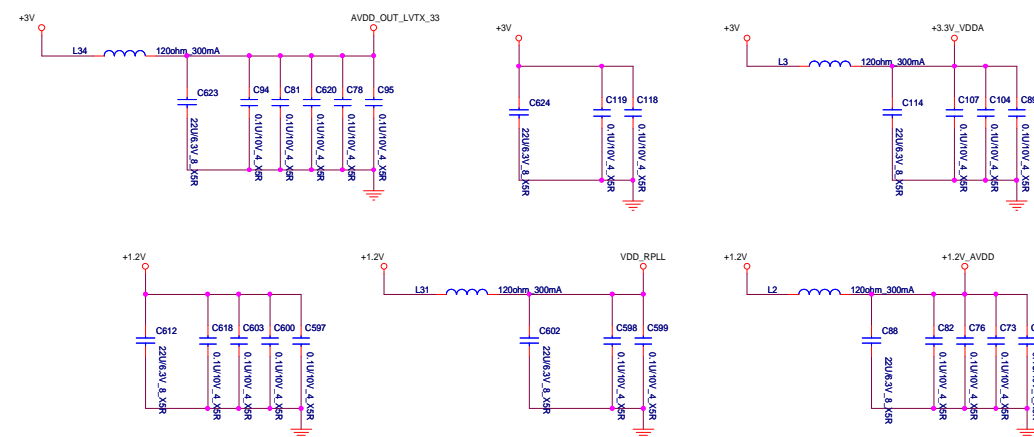


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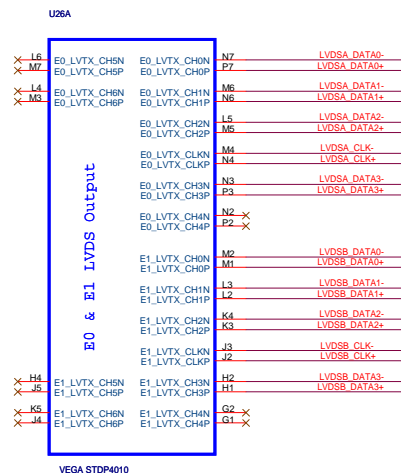
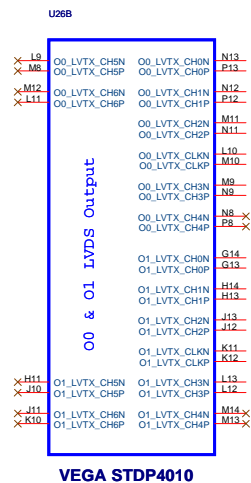


Net Name	Function	Value	Note
ST_I2S_WCLK_BS0	Pull low to GND	0	+3V0  4.7KJ 4 R537 ST_I2S_WCLK_BS0 4.7KF 4 R546 
ST_I2S_BCLK_BS1	Pull low to GND	0	+3V0  4.7KJ 4 R111 ST_I2S_BCLK_BS1 4.7KF 4 R105 
ST_I2S_0_BS2	IC_OSC_SEL 0 = TCLK from external source 1 = TCLK from internal ring oscillator	0	+3V0  4.7KF 4 R545 ST_I2S_0_BS2 4.7KJ 4 R544 
ST_I2S_1_BS3	TTL_LVDS_OUT 0 = Output is in LVDS format 1 = Output is in TTL format	0	+3V0  4.7KJ 4 R102 ST_I2S_1_BS3 4.7KF 4 R100 
ST_I2S_2_BS4	OCM_BOOT_SEL 0 = OCM boot from internal ROM 1 = OCM boot from external ROM/Flash	1	+3V0  4.7KF 4 R99 ST_I2S_2_BS4 4.7KJ 4 R98 
ST_I2S_3_BS5	Wide_Narrow_Bus 0 = LVDS_Dual / TTL_Single 1 = LVDS_Quad / TTL_Dual	0	+3V0  4.7KJ 4 R542 ST_I2S_3_BS5 4.7KF 4 R543 
ST_UART_TX_BS6	Pull low to GND	0	+3V0  4.7KJ 4 R110 ST_UART_TX_BS6 4.7KF 4 R104 
ST_AUX_UART_TX_BS7	I2C_DEV_ID 0 = RW: 0x6, 0xE7 1 = RW: 0xE4, 0xE5	0	+3V0  4.7KJ 4 R592 ST_AUX_UART_TX_BS7 4.7KF 4 R595 

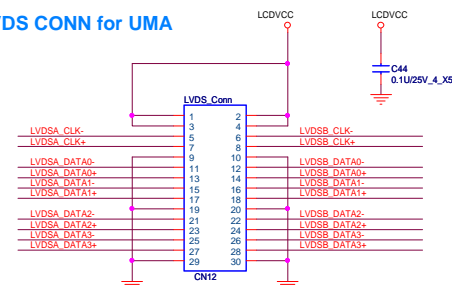
Rev B, R545 change to NU, R544 change to Stuff



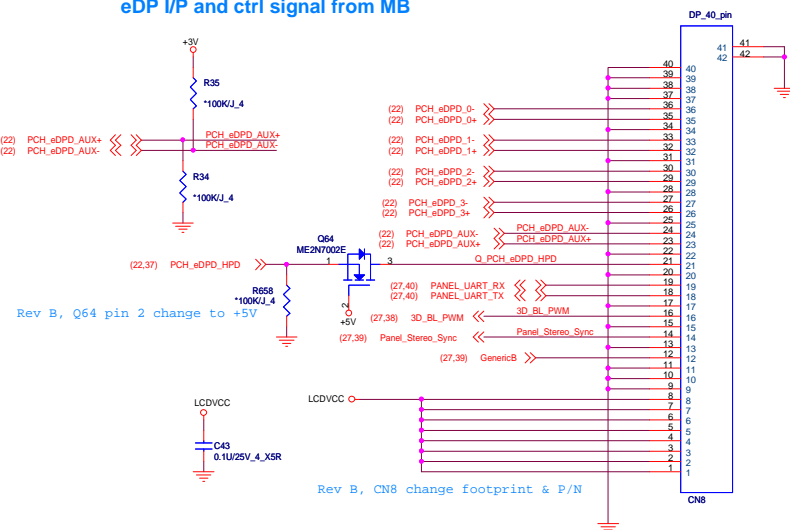
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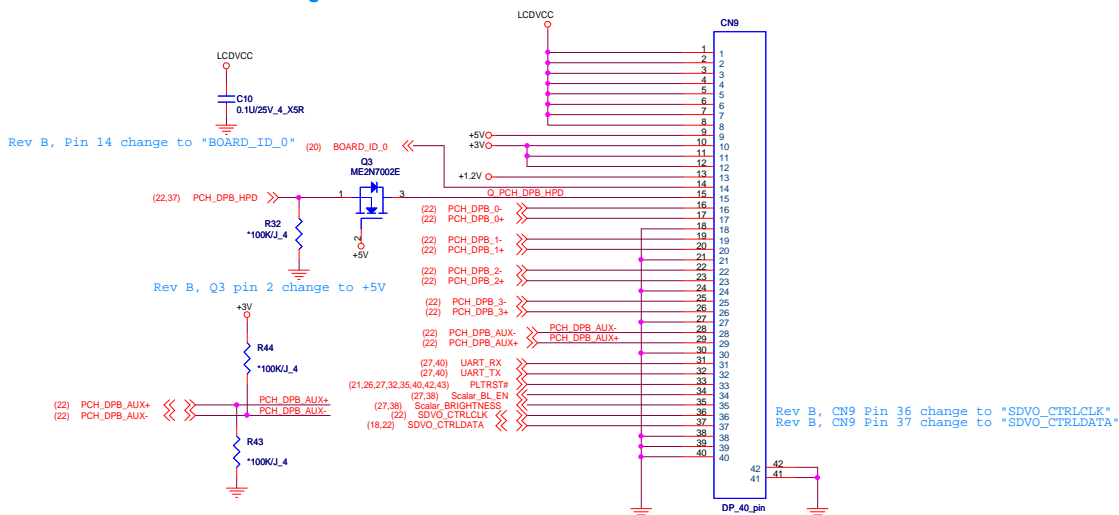
LVDS CONN for UMA



eDP I/P and ctrl signal from MB

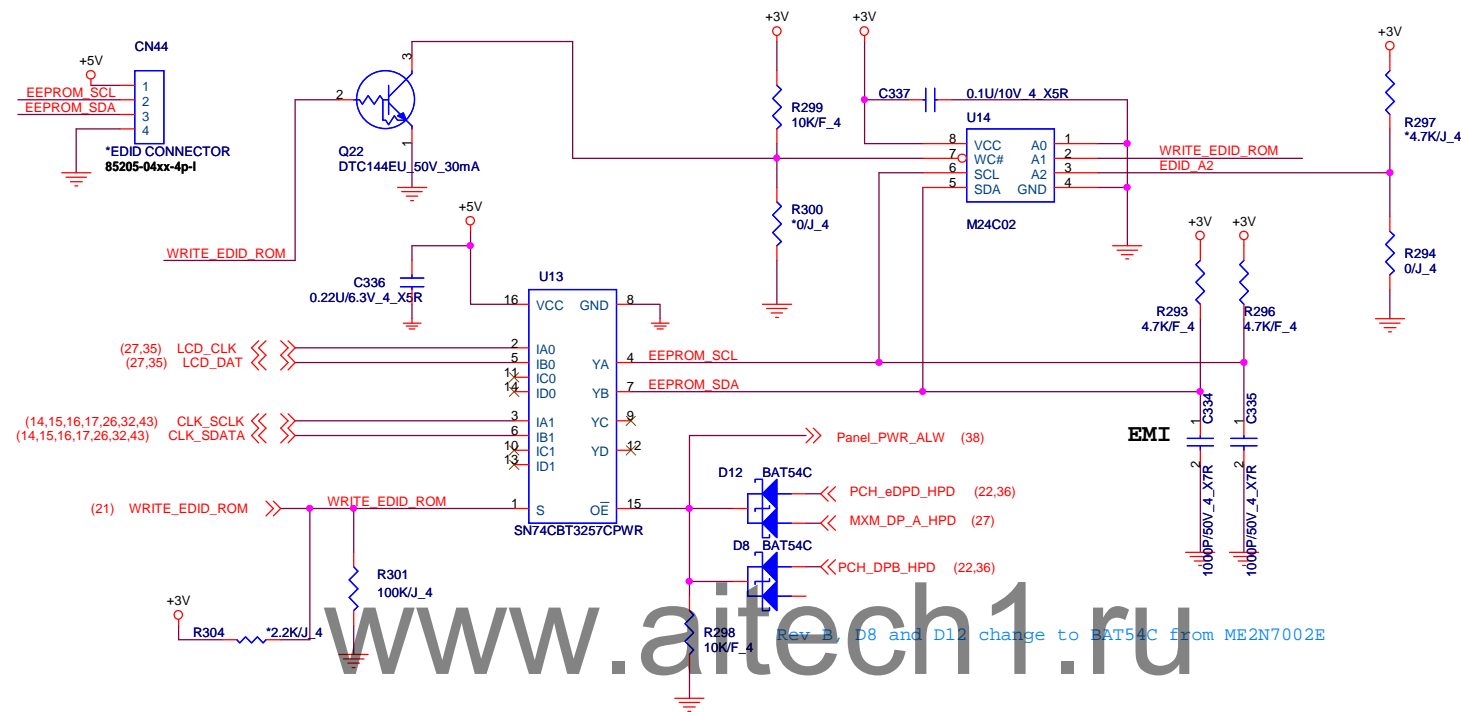


DP I/P and ctrl signal from MB

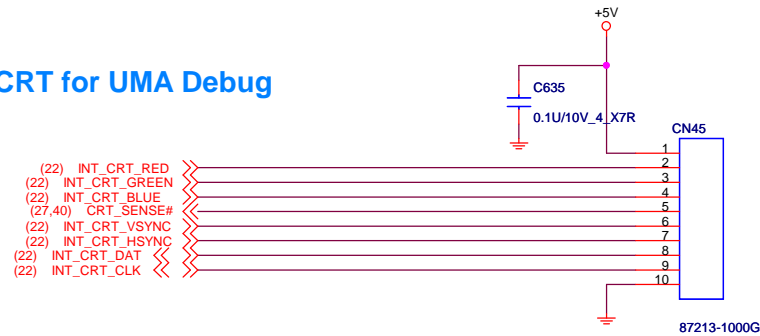


EEPROM IIC Selection

PANEL EDID DATA



CRT for UMA Debug



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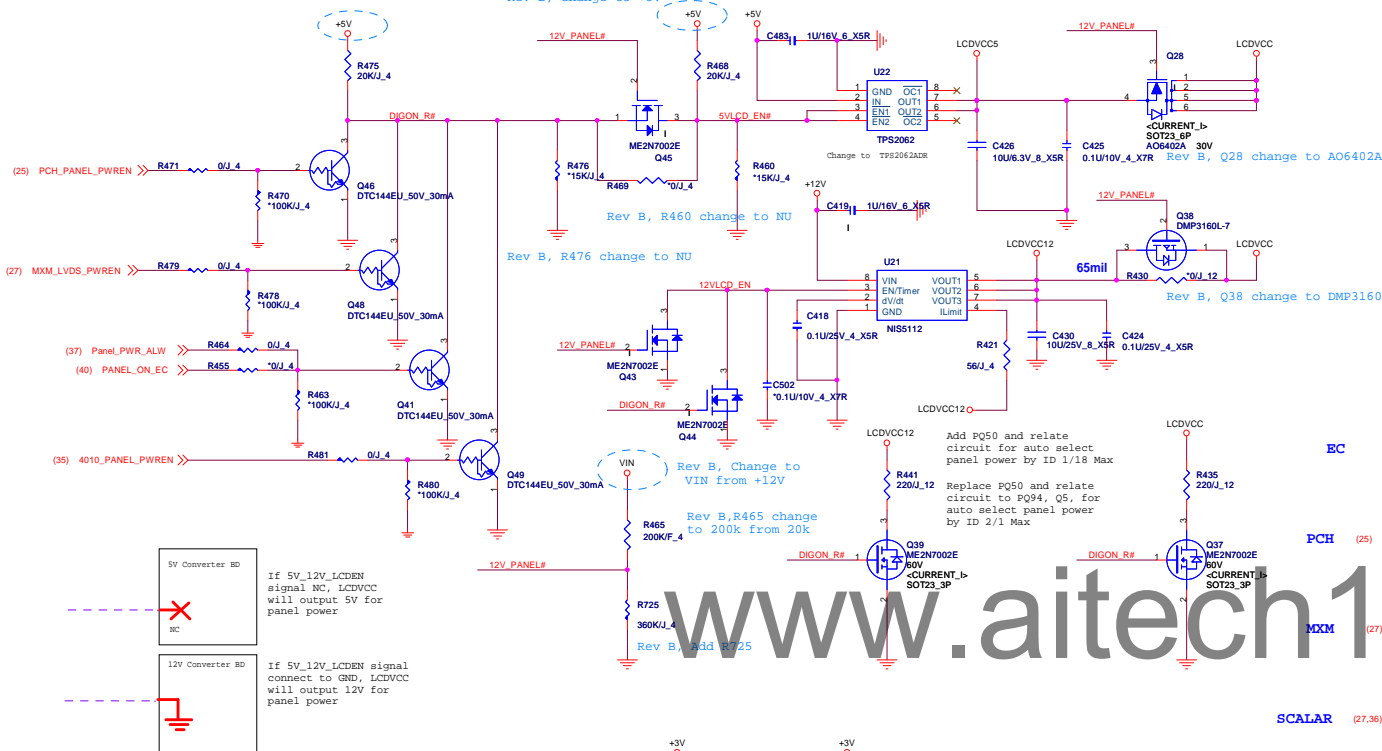
Quanta Computer Inc.
PROJECT : WJ1

Size	Document Number	Rev
	Panel (EDID)	B
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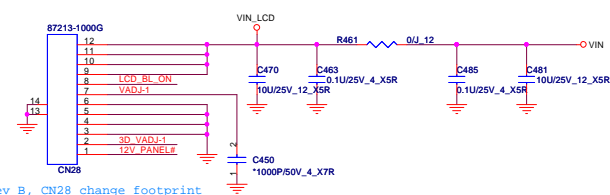
PANEL VCC CONTROL

Rev B, Change to +5V

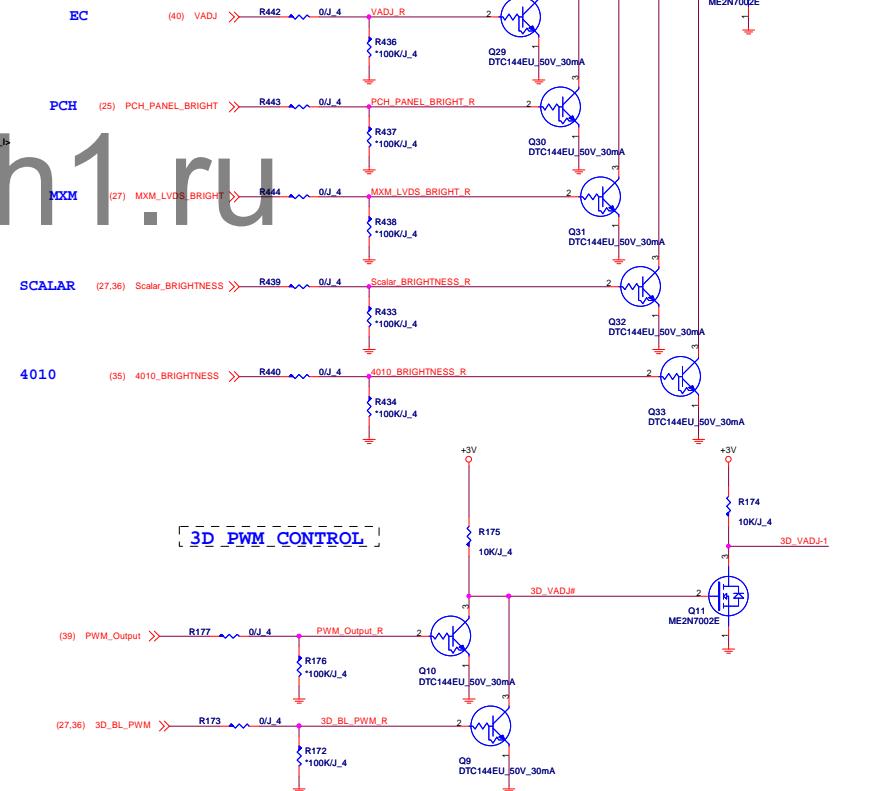
Rev B, Change to +5V



TO Converter Board

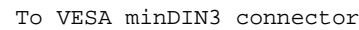


PWM CONTROL



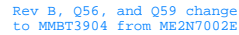
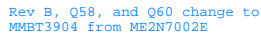
3D PWM CONTROL

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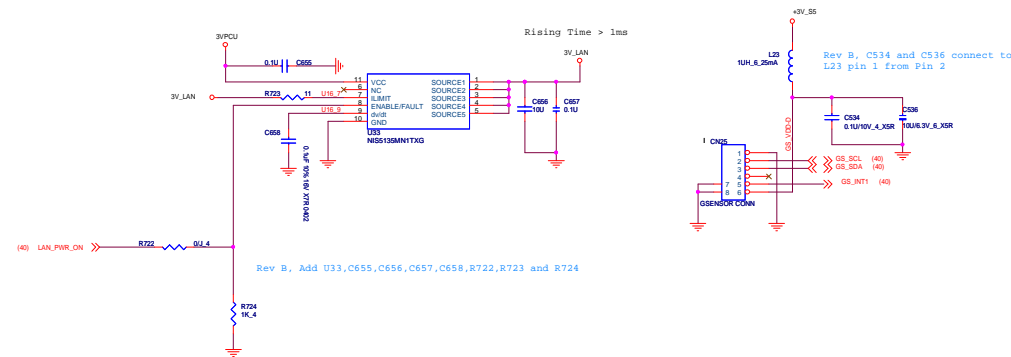
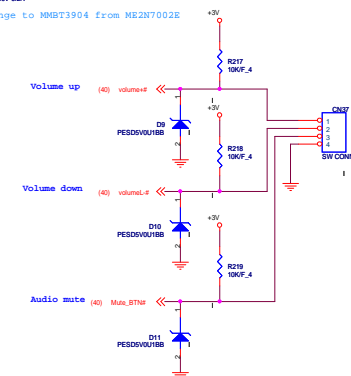
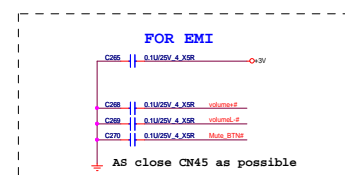
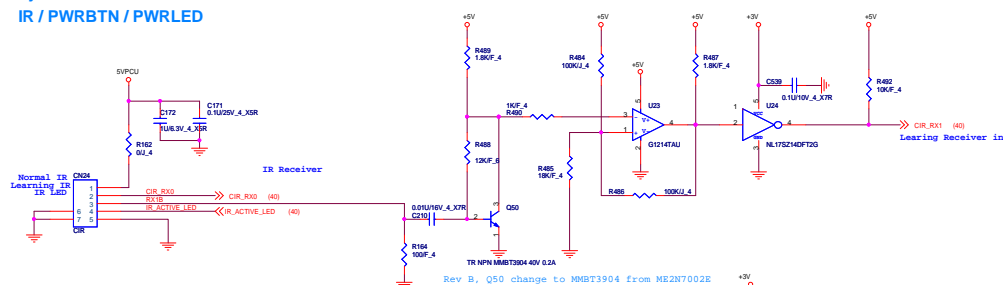
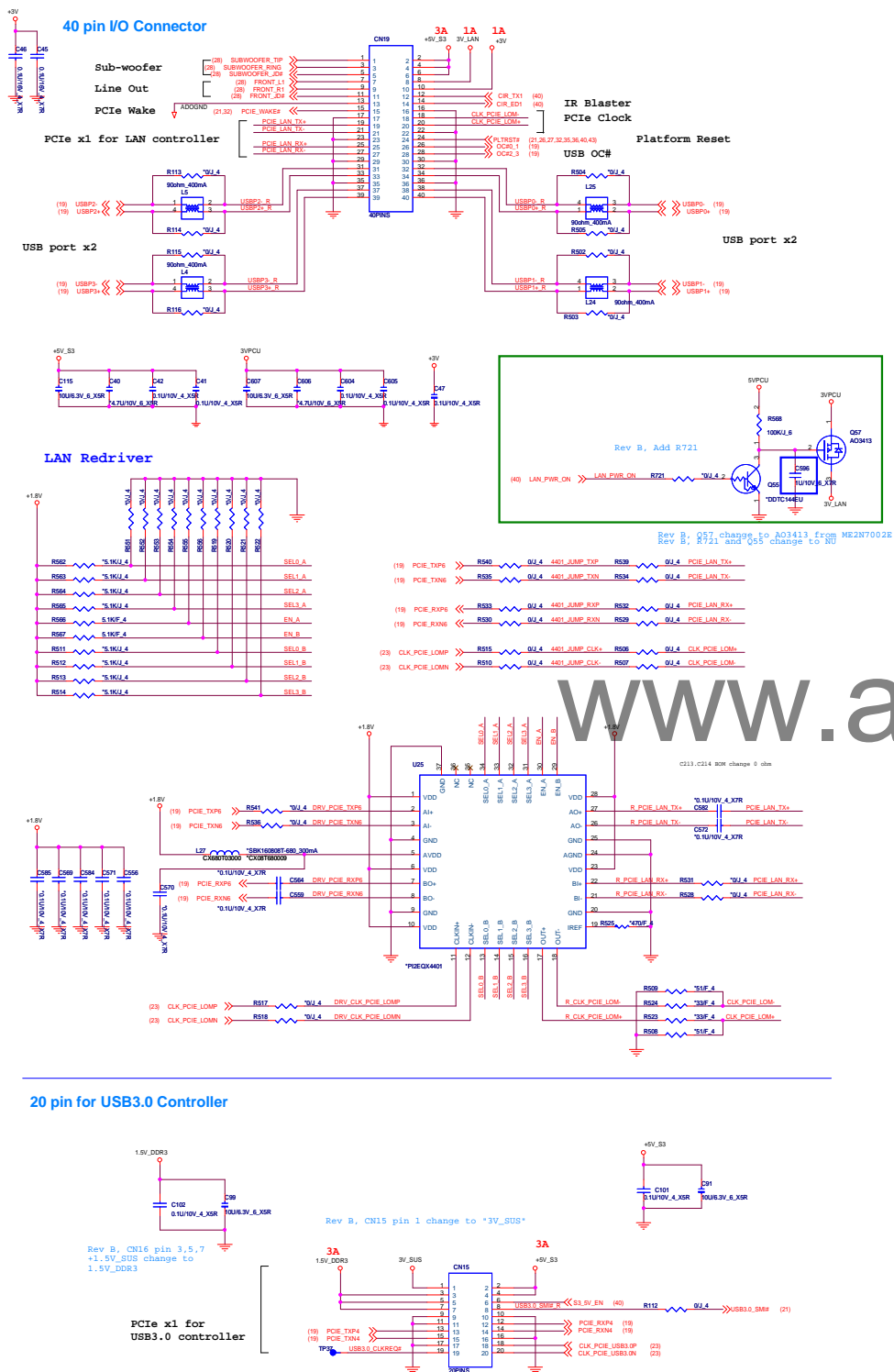


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Date:	Monday, October 18, 2010	Sheet 39 of 54

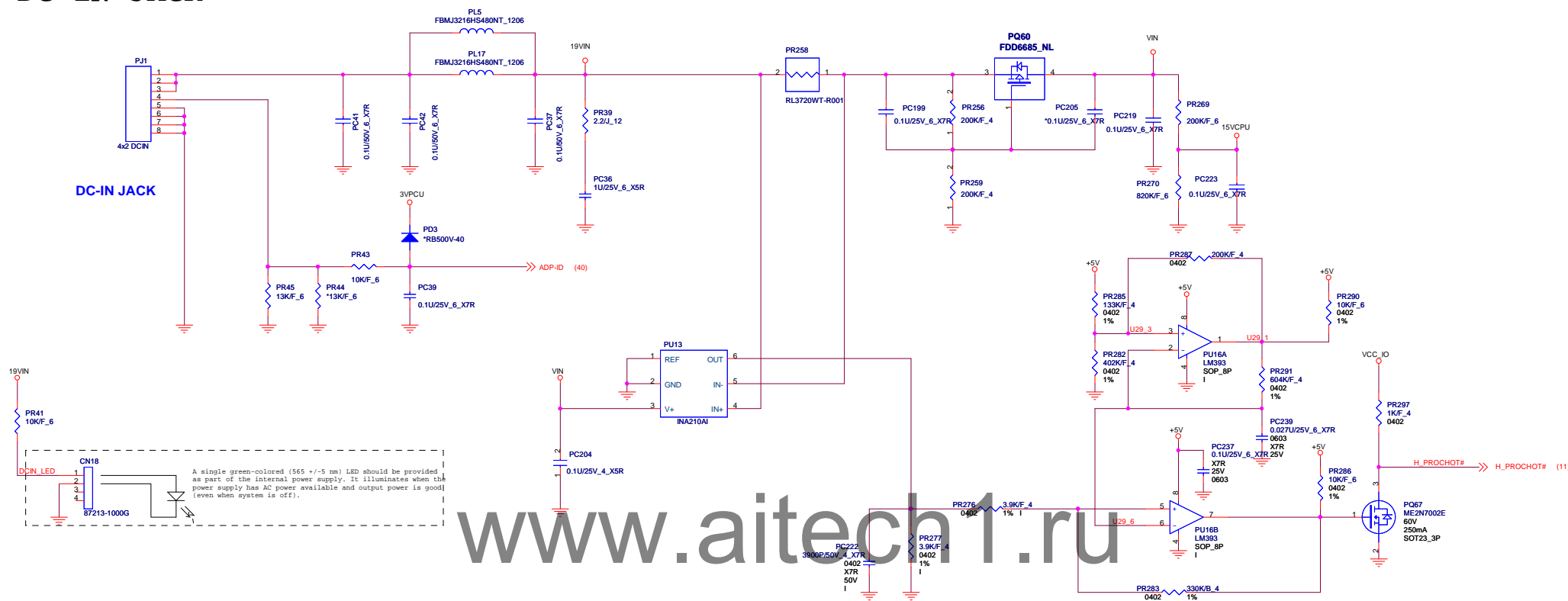


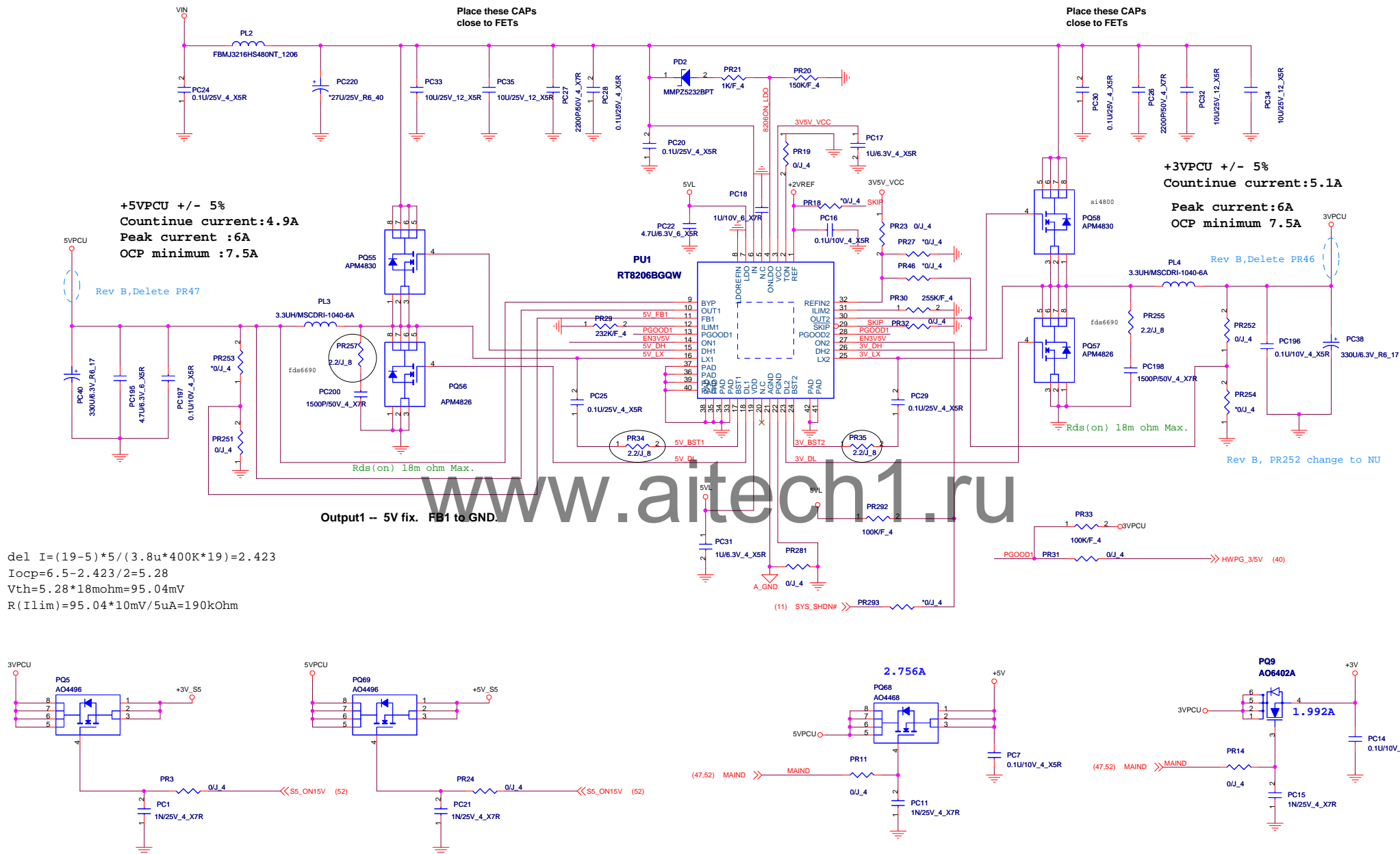


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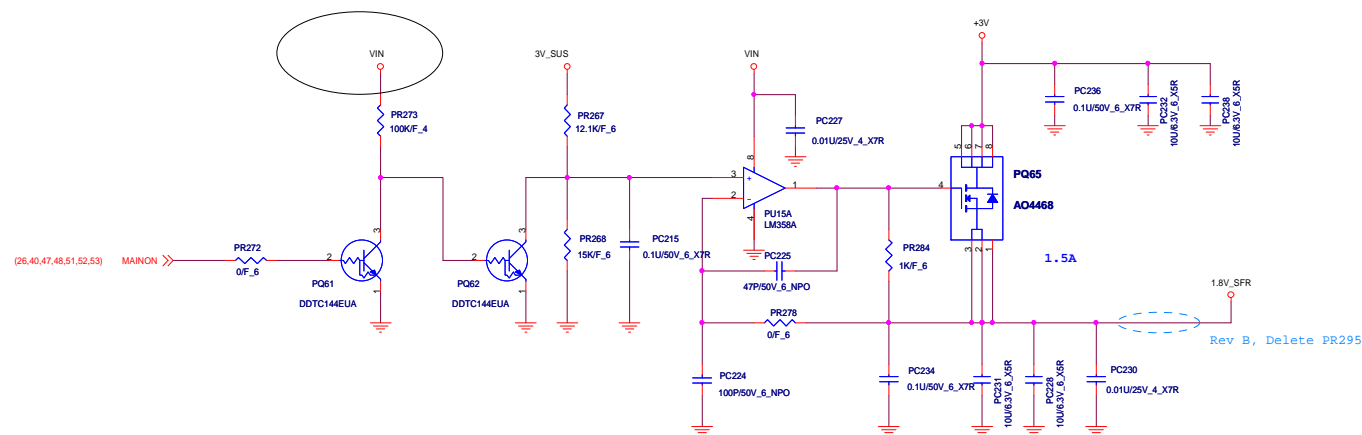



```
ramp-up time for all power rails
50 us <All power rails except 5V_S5 <40 ms
100 us <5V_S5<40 ms
```

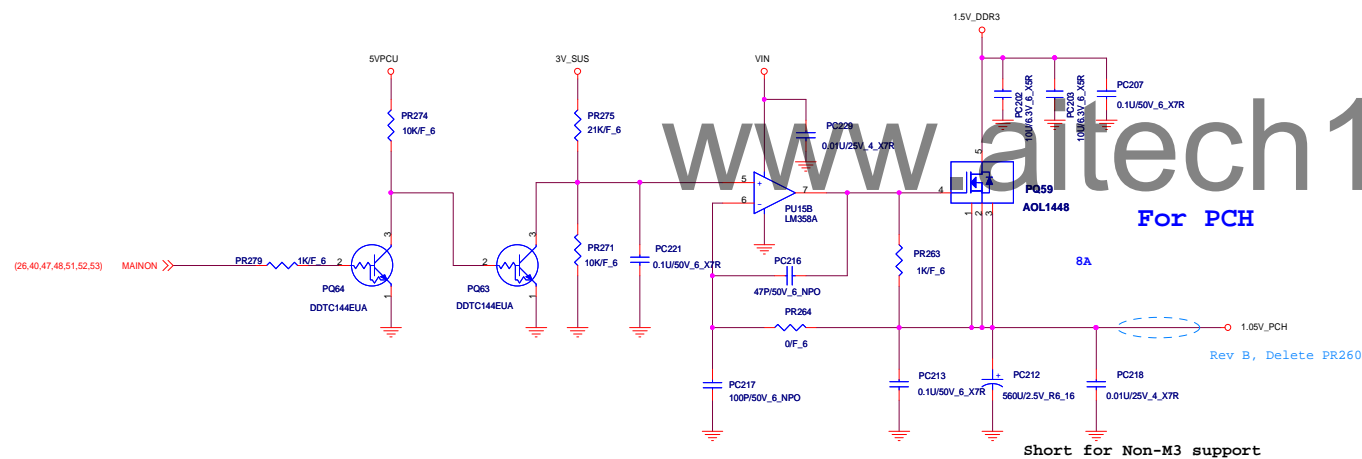




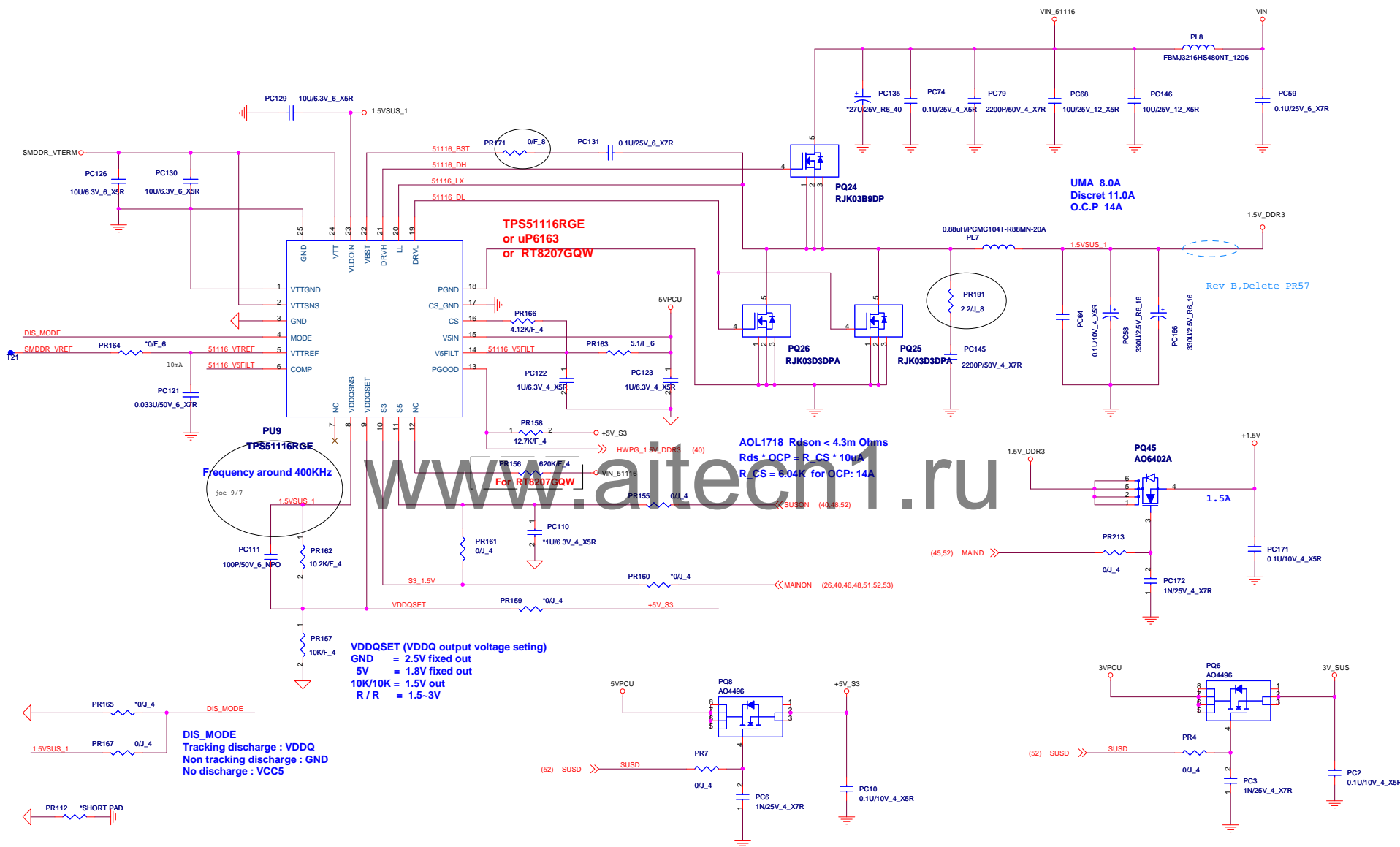
1.8V_SFR, 1.05V_PCH

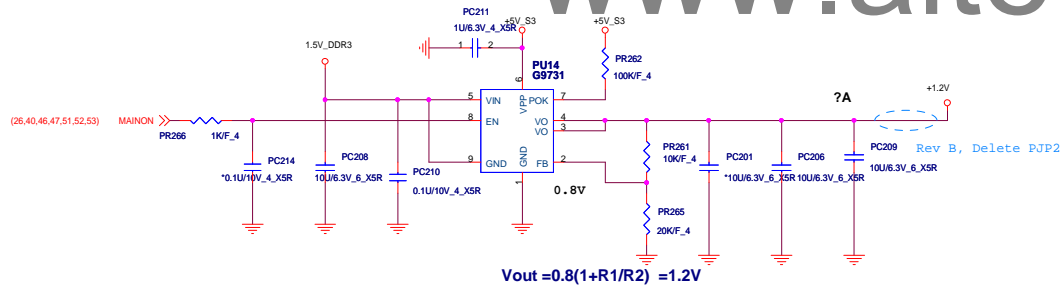
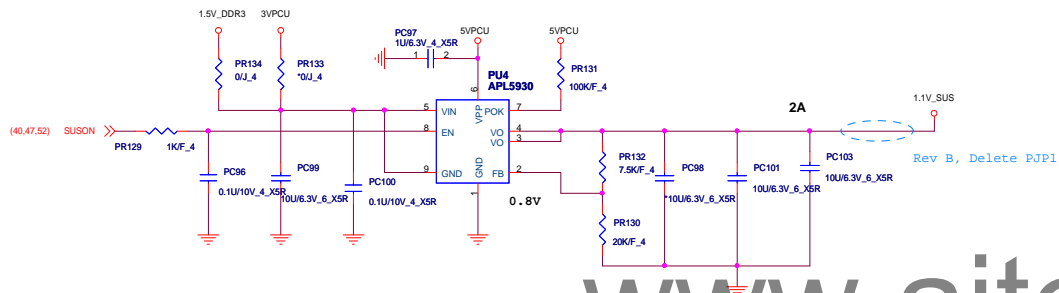
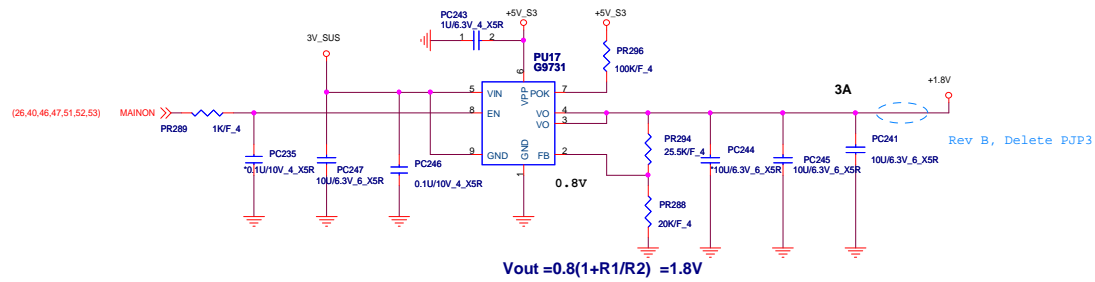


Main source:AL000358012
Second source:AL000358071

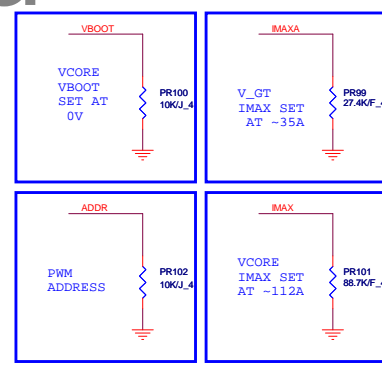


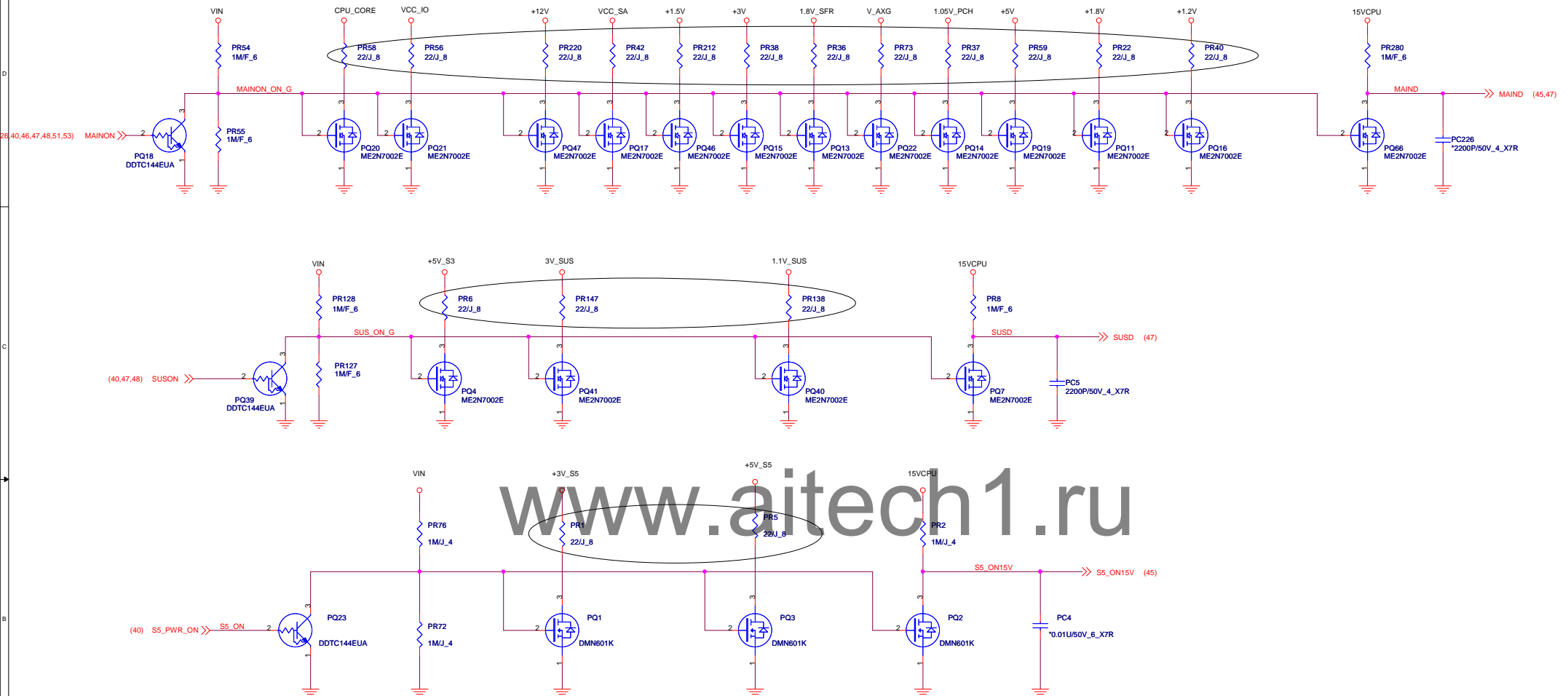
DDRIII-- 1.5VSUS





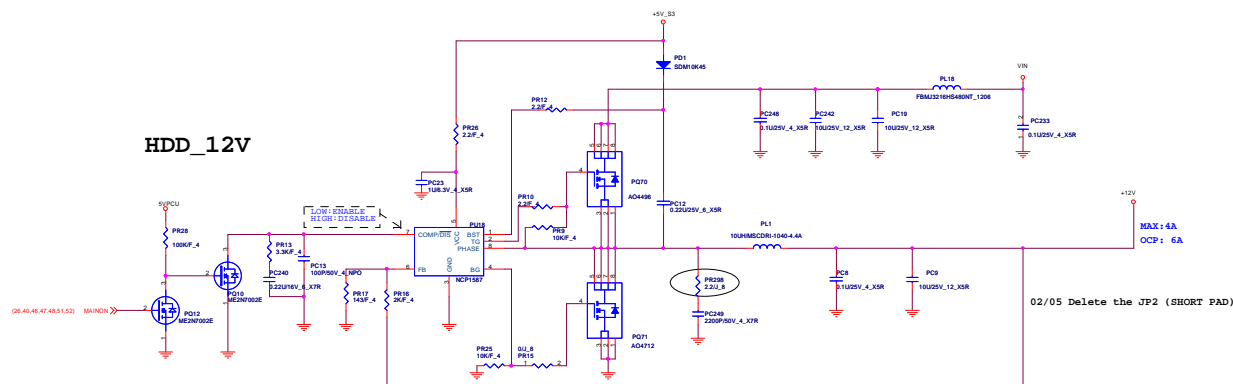
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EVT(Rev. A) to DVT(Rev. B)

Page 02, SATA HDD and SDD change to SATA Gen3 from Gen2
Page 11, R371 change to NU
R367 change to 120 ohm
Delete R366,R369,R381,R377,R382,R378,R344,
R376,R429,R370,R375,R374,R352,R373,R372,R348
Page 12, C394 change to Stuff
Add C648~C654

Page 19, U28 pin BP43 change to net "USB_OC4#"
U28 pin BJ41 change to net "USB_OC5#"
RP17 pin 8 connect to "USB_OC4#", pin 9 connect to "USB_OC5#"
RP17 pin 1,3,5,7 change to floating
Add L37,L39,L40
Delete C574 and C575

Page 20, R638 change to Stuff
R675,R677 and R681 pull up voltage change to +3V
U28 pin BR19 change to GPIO1
U28 pin BA22 change to BOARD_ID_0
U28 pin BR16 change to BOARD_ID_1
U28 pin BU16 change to GPIO68
U28 pin BM18 change to GPIO69
Add R726 and R727, NU

Page 21, R600 change to NU
Add R710,R711,R712 and R713
R701, U32 and C647 change to NU
R707, R604 change to Stuff
U30 change footprint
R19,R27, R54 and R659 pull up voltage change
to +3V_S5
R652 pull up voltage change to +3V_S5, NU
R655,R669, R662, R21 and R53 pull up voltage
change to +3V_S5
GPIO12 change to "EC_SMI#"
GPIO13 change to "EC_SCI#"
GPIO44 change ro "CLR_BIOS_DATA#"
GPIO45 change to "CLR_PASSWORD#"
SW1 change footprint
C642 and C643 change to 12p
Delete R629

Page 23, Delete RP1,R654
Page 24, Q2 and Q63 change to MMBT3904 from ME2N7002E
U28 pin AN52, VCCSPI change to +3V from +3V_S5
Delete R661, R649,R587 and R594

Page 26, Q67 and Q68 change to AO3413 from ME2N7002E
Q16 change to AO3413 from MF2N7002E
Q20 change to MMBT3904 from MF2N7002E
Add R708, R709 and R718,Q70

Page 27, CN7 change footprint & P/N
Add R728 and R729, NU
Add R733 and R734

Page 28, AR70 change to 0 ohm from 10 ohm
AD4 change footprint and Stuff
AR69, AR40 change to NU, AR71 change to Stuff
Change AC38,AC39,AC58,AC59,AC60 and AC61
AR41,AC66,AR43,AR42,AC67 and AR44 change to NU
Add AR90 and AR91

Page 31, F5 change to NU
Delete F1,F2,F3 and F4

Page 33, Delete USB3.0 Controller
Delete U8,R224,R254,R255,R256,R706,R236,C292,
C293,R226,R237,R235,R238,R255,R261,R270,
R267,R264,C332,U12,L12,C288,C286,C319,
C318,C316,C312,C317,C285,C302,C300,C289,
C307,C290,C326,C294,C308,C320,C314,C305,
C325,C315,C313,C287,C322,C311,C309,C291,
C310,C323,C327,C306,C321,R232,R233,L14,
U6,U5,R230,R231,L13,C296,C297,C298,C299,
U7,U4,R222,R227,R223,R281,R282,C304,R234,
C301,C295,R220,C303,C278,C276,C280,C284,
U11,R274
Change CN39 and CN40
Add F8,R735,R736 and C659

Page 34, Delete C331, R273, R275 and R228
Change R151 and R149
Add R740 and R741, R741 NU

Page 35, R94,R73,R91,R108,R107,R75,R88,R84,R57,R66,R545,R608 and R609 change to NU
R90, R123, R60, R63 and R544 change to Stuff
U29 change to 2M bits
C588 and C589 change to 15p
R608 and R609 change to NU
R482 change to U26 pin F11

Page 36, CN8 change footprint & P/N
Q64 pin 2 change to +5V
Q3 pin 2 change to +5V
CN9 pin 14 change to "BOARD_ID_0"

Page 37, D8 and D12 change to BAT54C from ME2N7002E
Page 38, Q38 change to DMP3160L from ME2N7002E
CN28 change footprint
Add R725
R465 change to 200K, R465 pin 1 change to VIN
R475 and R468 pull up voltage change to +5V
R476 and R460 change to NU
Q28 change to AO6402A
Add R738 and R739

Page 39, Q27 change to MMBT3906 from ME2N7002E
Page 40, Title Block change to ITE 8519E from ITE8512N
R325 and R326 change to NU
U15 pin 72 change to "VGA_TH_ALERT#" and change P/N
Add D26
D13 change to NU

Page 41, Q56,Q58,Q59 and Q60 change to MMBT3904 from ME2N7002E
Q12 change to MMBT3904 from ME2N7002E

Page 42, Q57 change to AO3413 from ME2N7002E
Q50 change to MMBT3904 from ME2N7002E
CN16 pin 3,5,7 "+1.5V_SUS" change to "1.5V_DDR3"
CN16 pin 1 change to "3V_SUS" from "+5V_S3"
Add U33,C655,C656,C657,C658,R721,R722,R723 and R724
R721 and Q55 change to NU

Page 43, R400 pin 1 change to "XDP_CPU_TRST_N" from "XDP_CPU_RST_N"
R651 change to 51 ohm, NU

Page 45, PL3 and PL4 change to 3.3uH
Delet PR46 and PR47
PR252 change to NU

Page 46, Delete PR295 and PR260
Page 47, Delete PR57
Page 48, Delete PJP1,PJP2,PJP3

Page 49, PC142 change to 1500pF
PC153 change to 3300pF
PC151 change to 150pF
PR198 change to 8.25k
PR195 change to 6.98k
PC148 change to 650pF
PR81 change to 100k
PC66 change to 150pF
PC147 change to 680pF
PR88 change to 7.5k
PR192 change to 5.49k
PR91 change to 34.8k

Page 50, PL13 change to 0.47uH
PC60 change to Stuff

Page 51, PL16 change
Add PC250 and PC251, PC252
Delete PR48 and PR250

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